WANGCO

A UNIT OF
PERKIN-ELMER DATA SYSTEMS

MODEL 511
MAGNETIC TAPE FORMATTER
NRZI
WITH P TYPE EMULATOR

OPERATION AND MAINTENANCE MANUAL

202195-001

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NRZI Formatter With Emulator (Model 511)
202195-001
Revision Level

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F	APPENDIX B Updated Write/Read Control PWB 201659 (G-H)	2/78

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SECTION 1

GENERAL DESCRIPTION

1.1 SCOPE

This manual describes operation and maintenance of the Model 511 Non-Return-to-Zero (NRZI) Magnetic Tape Formatter with P-type Emulator manufactured by WANGCO, Incorporated. The NRZI Formatter simplifies interfacing of magnetic tape units with digital computers. This manual is divided into the following six sections:

- Section 1: General Description
- Section 2: Installation and Interfacing
- Section 3: Operating Instructions
- Section 4: Theory of Operation
- Section 5: Maintenance and Troubleshooting
- Section 6: Logic Data

1.2 INTRODUCTION

The Model 511 NRZI Formatter (ref. Frontispiece) allows writing and reading of IBM- or ANSI-compatible 9-track or 7-track magnetic tapes. Nine-track data density is standard at 800 bits per inch (BPI), and 7-track data density is selectable at 200, 556, or 800 BPI.

NOTE

Throughout this manual all references to BPI is intended to relate directly to bits per 2.54 centimeters (cm).

1.2.1 FUNCTIONAL DESCRIPTION

Formatter control enables automatic performance of all major tape-unit operations and makes possible individual selection and operation of up to four daisy-chained Tape Units in a series parallel configuration. Tape Units for use with the Model 511 NRZI Formatter can be a mixture of any of the following configurations:

A. Seven-track or 9-track format
B. Any of two tape speeds (7-track)
C. Read/Write (single-stack) or Read-After-Write (dual-stack) head.

1.2.1.1 Control Functions. The 511 NRZI Formatter provides the following control functions:

A. Tape Unit motion control.
B. Cyclic Redundancy Check Character (CRCC) generation and checking.
C. Longitudinal Redundancy Check Character (LRCC) generation and checking.
D. Vertical Redundancy Check (VRC) generation and checking.
E. Inter-Record Gap (IRG) generation.
F. IBM-compatible file mark generation.
G. Status reporting of pertinent operational modes.

1.2.1.2 Timing. All critical clock and delay times are derived from a crystal-controlled oscillator; no single-shot multivibrators are used, and no calibrations or potentiometer adjustments are required in the Formatter or in the Emulator.

1.2.1.3 Emulator. The Emulator, mounted on the rear of the Formatter enclosure, provides a compatible interface between a Controller that uses a Pertec Input/Output (I/O) format and the standard WANGCO I/O format. This allows replacement of a standard Pertec NRZI Formatter with a WANGCO NRZI Formatter by using the existing Controller; however, the following three functions that are available with the Pertec Formatter are not available with the modified WANGCO Formatter:

A. No variable Erase function (only fixed Erase function).
B. No Edit function.
C. No external Write parity generation option. Parity for the Write function is generated by the Formatter.

1.2.1.4 Tape Speed. The Model 511 NRZI Formatter is compatible within the entire tape-speed range of 12.5 to 112.5 inches per second (ips) or 31.75 to 285.75cm/sec without change of crystals. Frequencies needed for tape speed are selectable by means of jumpers which can be changed in the field.

1.2.1.5 Additional Features. The Model 511 NRZI Formatter provides the following additional features:

A. Continuous Read or Write (On-the-Fly) operations at maximum tape speed without stopping in the IRG.
B. Writes and reads IBM-compatible file marks in 7-track or 9-track formats.
C. Special low-threshold data recovery circuit.

1.2.2 CONTROLS AND INDICATOR LAMPS

The following controls and indicator lamps are provided on the operator control panel (OCP) at the front of the Formatter (see frontispiece):

A. Slide switches allow any of the Tape Units (arbitrarily assigned letters of A, B, C, and D) to be assigned any of four possible addresses (0, 1, 2, or 3).
B. Lamp indication when Formatter is selected by the Computer.
C. Lamp indication of Tape Unit selected by the Computer.
D. Lamp indication of high or low density selection (7-track Tape Units; or for Tape Units with Remote Density option, the lamps indicate PE or NRZI selections respectively).
E. Lamp indication of odd or even parity selection (7-track Tape Units only).
F. Remote or Manual control for density and parity selection (7-track Tape Units only; 9-track Tape Units are always 800 BPI and odd parity).
G. Illuminated pushbutton power switch.

1.3 PHYSICAL DESCRIPTION

1.3.1 MOUNTING

The Formatter mounts in a standard 19-inch (48.26cm) EIA or RETMA equipment rack. The front panel is 5.25 inches (13.335cm) high, hinged at the left side, and secured by a 1/4-turn latch. Opening the front panel provides easy access for removal of the printed wiring board (PWB) assemblies. Formatter depth is 21.5 inches (54.61cm), but an additional two inches should be allowed for an input/output (I/O) cable service loop. The Formatter weighs approximately 25 pounds (11.33975kg).

1.3.2 CONNECTIONS

Cable connections are made at the rear of the Formatter, using circuit-board-edge connectors on which circuit-board-type cable terminators are connected. The connector for interfacing the Formatter with the customer-furnished Controller and the complete I/O cable assembly for Tape Unit-Formatter interface are provided as standard equipment, but the daisy-chain cable assembly is optional.

1.3.3 SERVICE ACCESS

Removal of pan-head screws from the top and bottom covers releases the covers and affords easy access to components on the PWB assemblies.

1.4 SPECIFICATIONS

Specifications for the WANGCO Model 511 NRZI Formatter are listed in Table 1-1.

TABLE 1-1. Model 511 NRZI Magnetic Tape Formatter Specifications (continued)

GENERAL	
Parameter	Characteristics
Tape Speed:	12.5 to 112.5 ips (31.75 to 285.75 cmps) with single crystal. Continuous Read or Write if desired (no stop in IRG).
Inter-Record Gap –	
9-Track:	0.6-inch (15.24 mm) nominal, 0.54-inch (13.716 mm) minimum.
7-Track:	0.75-inch (19.05 mm).
Circuitry:	Silicon semiconductors
Interface Voltages –	
Low:	0.0 ±0.4V } Compatible with DTL 900 Series
High:	3.9 ±1.5V } or TTL 7400 Series
Tape Format Compatibility –	
9-Track:	800 BPI } ANSI- or IBM-compatible
7-Track:	200, 556, or 800 BPI }
Magnetic Tape Units per Formatter:	Up to 4 (in daisy-chain configuration). Tape Units may be mixed; and 2 speeds (7-track only), single-stack or dual-stack head. Switchable assignment of Tape Units to Computer (by number) without changing electrical connectors.
Functions Controlled:	Tape motion, generation of CRCC, LRCC, VRC, IRG and IBM-compatible file marks.
Lamp Indications:	Power on; Formatter selected; Tape Unit selection; density selection; parity selection.
Remote/Manual Selection:	Switch allows remote or manual control for density and parity selection.

TABLE 1-1. Model 511 NRZI Magnetic Tape
Formatter Specifications (concluded)

PHYSICAL	
Parameter	Characteristics
Dimensions – Height: Width: Depth:	 5.25 inches (13.335 cm). 19 inches (48.26 cm). 21.5 inches (54.61 cm).
Approximate Weight:	25 pounds (11.34 kg).
Mounting:	3 vertical spaces in standard 19-inch (48.26 cm) EIA or RETMA equipment rack.
Power:	110, 115, 120, 125, 220, 230, 240 or 250 VAC ±10% (selectable by transformer tap). 100 or 200 VAC ±10% available as special option. 160W maximum, 48–62 Hz.
ENVIRONMENTAL	
Parameter	Characteristics
Operating Temperature:	0 to 50° C (32 to 122° F).
Storage Temperature:	–40 to +75° C (–40 to +167° F).
Altitude:	Sea level to 20,000 feet (6097.5 meters).
Relative Humidity:	10 to 95% (noncondensing).

SECTION 2

INSTALLATION AND INTERFACING

2.1 GENERAL

This section provides information for unpacking, inspecting, installing, and interfacing the WANGCO Model 511 NRZI Magnetic Tape Formatter.

2.2 UNPACKING AND INSPECTION

Use the following procedure when unpacking and inspecting the Formatter:

A. Remove contents of shipping container and inspect for in-transit damage. If damage is evident, notify the carrier and the manufacturer. Specify nature and extent of damage.

B. Verify contents of shipping container agree with shipping list. Notify a WANGCO representative if there are any shortages.

C. Verify that Formatter model designation and serial number agree with those on the shipping invoice.

D. Open the front panel of the Formatter by turning the 1/4-turn latch at the right side, then use the white nylon card extractors attached to each side of each major assembly board and remove the boards.

NOTE

Circuit board components are reference designated by means of a coordinate system, with letters at the left side of the board and numerals across the top.

E. Inspect major assemblies for loose hardware. Tighten hardware where necessary.

F. When reinserting the circuit boards, verify they are firmly seated in the rear panel sockets; otherwise the front panel cannot close nor can the Formatter operate properly.

2.3 MOUNTING

A small packet of mounting hardware that contains the 10-32 Phillips-head screws, metal grommets, and nylon chafing guards is included with each NRZI Formatter. The Formatter is rack mounted by aligning its four mounting holes with four threaded mounting holes in the rack and securing it with the mounting hardware.

2.4 ACCESS

The front panel of the Formatter is hinged on the left side. During installation, provision should be made for at least 18 inches (45.72cm) of front-panel clearance to allow circuit board removal and access for other maintenance purposes. Access space should also be provided at the rear of the Formatter for servicing and cable interconnections shown in Figure 2-1.

2.5 COOLING

A fan within the Formatter provides all necessary cooling; however, airflow restriction about the sides and the perforated top and bottom covers should be avoided. The fan is at the left front of the Formatter (ref. figure 2-1) and directs air back across the power supply. The air then flows to the right, across the circuit boards, and exits primarily from the top and rear of he Formatter.

2.6 CABLING

A diagram of NRZI Formatter cabling configuration is shown in Figure 2-2. The following three cables are essential for system operation:

A. Power cable.
B. I/O cable (Formatter-to-Tape Unit).
C. I/O cable (Formatter-to-Controller).

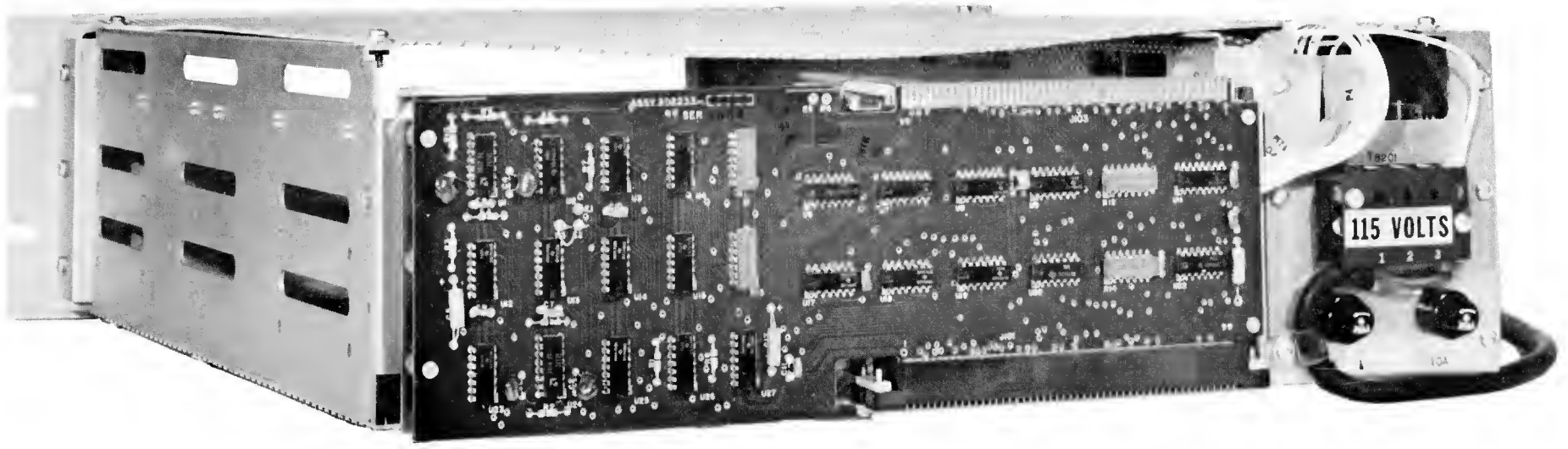


Figure 2-1. Formatter, Rear View

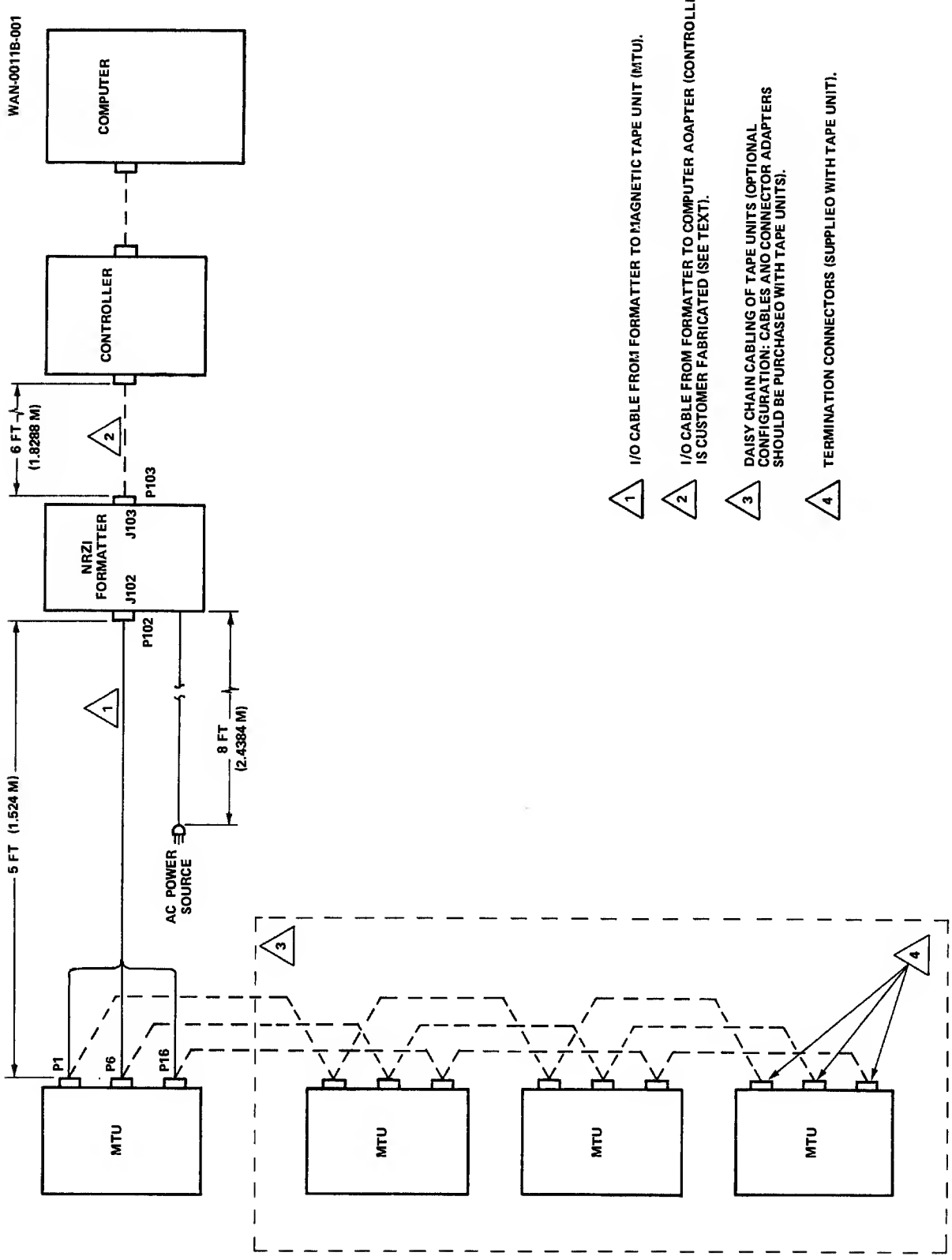


Figure 2-2. Formatter Cabling Configuration

2.6.1 POWER CABLE

A three-pin power cable, terminated in a three-pin plug (one pin is ground), is an integral part of the Formatter. The power source must be located within the eight-foot (2.4384m) length of the cable. The power-cable plug and power-cable terminal-board cover are labled with the AC voltage required for proper operation of the Formatter. Power transformer terminals are internally strapped at the factory, as specified by purchase order (ref. table 1-1 for power options). A decal on the rear left side of the Formatter chassis shows transformer strapping connections for various power configurations.

CAUTION

BEFORE CONNECTING THE AC LINE PLUG ON THE FORMATTER POWER CABLE TO THE POWER SOURCE, VERIFY THAT SOURCE VOLTAGE CONFORMS TO THAT SPECIFIED ON THE DECAL ATTACHED TO THE FORMATTER REAR PANEL.

2.6.2 I/O CABLE (FORMATTER-TO-TAPE UNIT)

This I/O cable is supplied with the Formatter. It is five feet (1.524m) long, and consists of a ribbon-type twisted pair, terminated on the Formatter end in a 100-pin circuit-board-edge connector (P102). From P102, the cable is split into three separate cables, each terminated in a 36-pin circuit-board-edge connector (P1, P6, and P16) for hookup with corresponding connectors on the associated Tape Unit When making system installation, Formatter and Tape Unit must not be separated by a distance greater than the length of this cable (ref. figures 2-1 and 2-2).

The three connectors on the Tape Unit end of MTU Cable Assembly 201336 must be attached to the Tape Unit in accordance with the following procedure:

CAUTION

DO NOT DEVIATE FROM THIS PROCEDURE OR EQUIPMENT DAMAGE MAY RESULT.

A. Connector P16 connects to jack J16. Verify that pin A (stamped on the connector) of P16 mates with pin A (etched finger) of J16 on the circuit board.

B. Connector P6 connects to jack J6. Verify that pin A of P6 mates with pin A of J6.

C. Connector P1 connects to jack J1. Verify that pin A of P1 mates with pin A of J1.

NOTE

If Tape Units are to be daisy-chained, total length of interconnecting I/O cables must not exceed 20 feet (6.096 m). The daisy-chain configuration requires the use of special connectors and additional cables for the Tape Units which should be ordered when Tape Units are purchased.

Two terminators (Control/Write) are supplied with each WANGCO Tape Unit. These terminators must be installed in the last Tape Unit in the daisy-chain. Termination for the Read lines is incorporated within the Formatter.

2.6.3 I/O CABLE (FORMATTER-TO-CONTROLLER)

This I/O cable is customer-fabricated, and uses the supplied 100-pin circuit-board-edge connector P101. Its length should not exceed 6 feet (1.83m), and it should be made of 22-26 AWG twisted-pair wires. Each twisted pair should have at least one twist per inch and a minimum insulation thickness of 0.01-inch (0.254mm). The ground wire of each twisted pair should be connected to ground as close to the origin or destination of the signal as possible (within six inches (15.24cm) maximum) to minimize ground-loop currents or cross-talk effects.

NOTE

If two Formatters are daisy-chained to the Controller, neither I/O cable length should exceed six feet (1.83m).

2.7 INTERFACING

The following information is necessary to provide correct interfacing between the Formatter, Controller, and Tape Units.

2.7.1 LOGIC LEVELS

The following two logic levels are used in the Formatter interface:

Low level — 0.0 ±0.4 VDC
High level — +3.9 ±1.5 VDC

NOTE

Throughout this manual, a bar over a logic term (e.g., $\overline{\text{BOT}}$) indicates the term is at a low level when active. Conversely, a term with no bar (e.g., RDS) is at a high level when active.

2.7.2 CABLE DRIVERS AND RECEIVERS

The cable drivers and receivers of the Formatter are shown in Figure 2-3. Observe that, with a high-level logic input, the configuration of the cable termination presents the equivalent of an open circuit to the Formatter.

2.7.2.1 Output Signals. All output signals from the Formatter are generated by low-active, open-collector integrated circuits capable of sinking 25 milliamperes (mA). This allows the Formatter output signals to be terminated to +5 Volts with resistors.

2.7.2.2 Input Signals. All input signals to the Formatter should be generated by drivers capable of sinking 30 mA when at the low-active level. These drivers need not supply any current when at the high level because resistor terminations are supplied at the receivers of the Formatter. The drivers need not be open-collector types either, because no wired OR input functions are used.

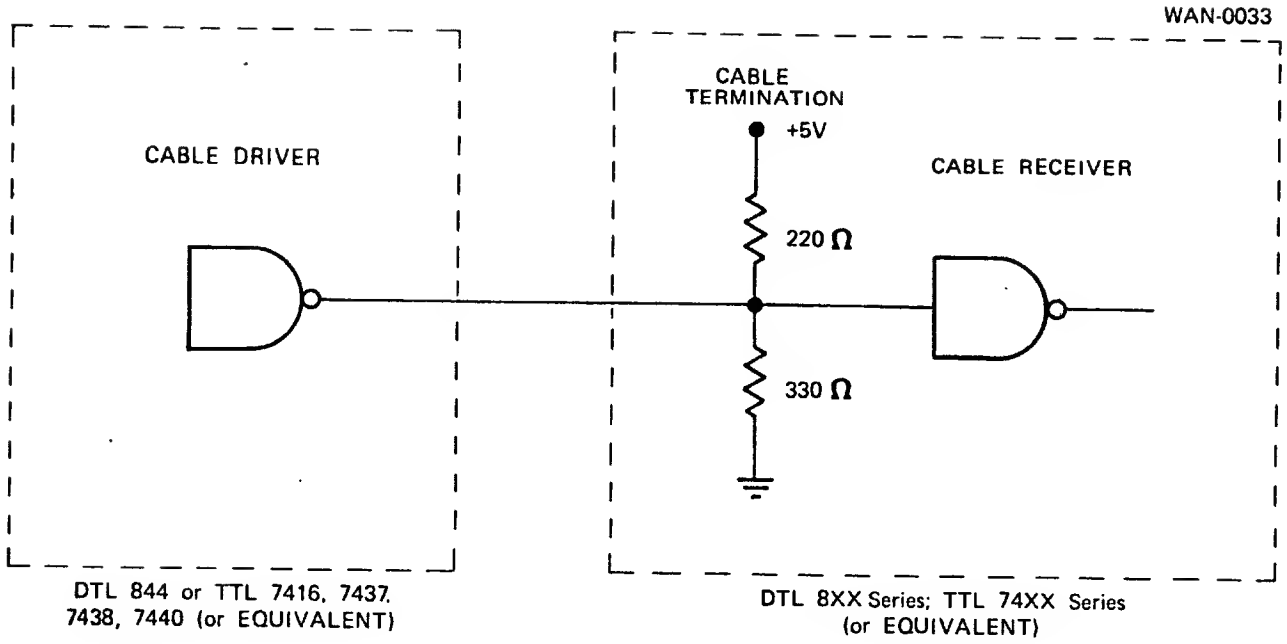


Figure 2-3. Cable Drivers and Receivers at Formatter Interfaces

2.7.3 FORMATTER-TO-TAPE UNIT INTERFACE

Table 2-1 lists the Formatter-to-Tape Unit I/O cable interface pin assignments. Terms under bars are low (0V) when active; terms without bars are high (+5V) when active. There are 24 signal lines from the Formatter to the Tape Unit which are grouped into three functional categories:

A. Address
B. Control
C. Write Data

2.7.3.1 Tape Unit Address. Four lines, SLCTA through SLCTD, are used to select Tape Units 0, 1, 2, or 3, respectively, when the Unit Select switches are arbitrarily set to A=0, B=1, C=2, and D=3. Each of these four lines is gated with the Formatter address signal to select one of the daisy-chained Tape Units. The Formatter decodes the S1 and S2 address lines from the Controller for this operation.

2.7.3.2 Control

Ten Control lines, SFC through WARS (ref. paragraphs 2.7.3.2.1 through 2.7.3.2.10) activate the selected Tape Unit when it is READY and ON LINE.

2.7.3.2.1 $\overline{\text{SFC}}$ – Synchronous Forward Command. A level which when low, causes the selected Tape Unit to ramp up to speed and drive forward at the rated speed. When switched to the high level, the Tape Unit ramps down to halt.

2.7.3.2.2 $\overline{\text{SRC}}$ – Synchronous Reverse Command. A level which when low, causes the selected Tape Unit to ramp up to speed and drive at the rated speed in the reverse direction. When switched to the high level, the Tape Unit ramps down to a halt.

2.7.3.2.3 $\overline{\text{RWC}}$ – Rewind Command. A negative-going pulse which causes the selected Tape Unit to rewind to the load point.

2.7.3.2.4 $\overline{\text{OFC}}$ – Off-Line Command. A negative-going pulse which causes the selected Tape Unit to revert to manual control. The Tape Unit must then be manually placed ON LINE before it can again be operated under remote control.

TABLE 2-1. Formatter/Tape Unit I/O Cable Interface

J102 Pin	Formatter to Tape Unit		J102 Pin	Tape Unit to Formatter	
60	$\overline{\text{SLCTA}}$	Tape Unit Address	64	$\overline{\text{RDY}}$	Status
53	$\overline{\text{SLCTB}}$		66	$\overline{\text{ONL}}$	
58	$\overline{\text{SLCTC}}$		62	$\overline{\text{RWD}}$	
54	$\overline{\text{SLCTD}}$		70	$\overline{\text{FPT}}$	
			57	$\overline{\text{LDP}}$	
			41	$\overline{\text{EOT}}$	
			76	$\overline{\text{NRZ}}$/PE	
			78	$\overline{\text{SINGLE}}$/DUAL	
34	$\overline{\text{SFC}}$	Control	80	$\overline{\text{LOW}}$/HIGH	
56	$\overline{\text{SRC}}$		72	$\overline{7\ \text{TRACK}}$/9 TRACK	
36	$\overline{\text{RWC}}$		74	$\overline{\text{DDI}}$	
55	$\overline{\text{OFC}}$				
44	$\overline{\text{SWS}}$				
8	$\overline{\text{OVW}}$				
46	$\overline{\text{DDS}}$				
94	$\overline{\text{THR1}}$				
92	$\overline{\text{THR2}}$				
43	$\overline{\text{WARS}}$				
			24	$\overline{\text{RDP}}$	Read Data
			14	$\overline{\text{RD0}}$	
		Write Data	32	$\overline{\text{RD1}}$	
45	$\overline{\text{WDS}}$	Strobe	18	$\overline{\text{RD2}}$	
			20	$\overline{\text{RD3}}$	
			28	$\overline{\text{RD4}}$	
			30	$\overline{\text{RD5}}$	
			10	$\overline{\text{RD6}}$	
48	$\overline{\text{WD0}}$	Write Data	12	$\overline{\text{RD7}}$	
50	$\overline{\text{WD1}}$				
51	$\overline{\text{WD2}}$		6	$\overline{\text{RDS}}$	Read Data Strobe
49	$\overline{\text{WD3}}$				
52	$\overline{\text{WD4}}$				
37	$\overline{\text{WD5}}$				
38	$\overline{\text{WD6}}$				
42	$\overline{\text{WD7}}$				
40	$\overline{\text{WDP}}$				

NOTE

OFC can be transmitted to a Tape Unit that is rewinding, even though the Tape Unit status indicates NOT READY.

2.7.3.2.5 $\overline{\text{SWS}}$ – Set Write Status. A level which when low, sets the selected Tape Unit from the Write mode to the Read mode within 20 microseconds if any of the following conditions occur: an $\overline{\text{SFC}}$, $\overline{\text{SRC}}$, $\overline{\text{RWC}}$, or $\overline{\text{ORC}}$ signal is received, the Tape Unit is manually switched to Off-Line, or interlock is lost. The Read mode is maintained until the next SFC or SRC is initiated.

2.7.3.2.6 $\overline{\text{OVW}}$ – Overwrite. The $\overline{\text{OVW}}$ signal is a level which causes the Tape Unit Write current enable/disable to ramp on and off to minimize rate of change of recorded inter-block gap magnetism when rewriting a record in the Edit mode. This signal level also causes the Write current and DC Erase Head current to be turned off immediately after rewriting the new record to prohibit erasing the beginning of the next record (ref. paragraph 2.7.3.2.10).

2.7.3.2.7 $\overline{\text{DDS}}$ – Density Select Line. This signal is used to select the packing density on 7-track Tape Units or to select NRZI Data Electronics on Tape Units equipped for dual-density operation. Low = High Density Selected (or PE), High = Low Density Selected (or NRZI).

2.7.3.2.8 $\overline{\text{THR1}}$ – Read Threshold 1. A level which when low, provides a high-threshold Read mode for marginal checking of written records on a Tape Unit that has a single-stack (Read/Write) head. This operation is usually accomplished by backspacing over a newly written record and then reading forward in the high-threshold Read mode to perform a parity check.

2.7.3.2.9 $\overline{\text{THR2}}$ – Read Threshold 2. A level which when low, provides an extra low threshold (on Tape Units appropriately equipped) for recovery of very-low-quality signals.

2.7.3.2.10 $\overline{\text{WARS}}$ – Write Amplifiers Reset. This signal controls the early turn-off of the Write and Erase currents after rewriting a record in the Edit mode (ref. paragraph 2.7.3.2.6). The negative-going transition of this signal initiates the Write/Erase current turn-off. This signal also generates the LRCC.

2.7.3.3 Write Data

Write Data signals ($\overline{WDP}$ and $\overline{WD0}$ through $\overline{WD7}$) are sent to the selected Tape Unit along with timing signals of the Write Data Strobe ($\overline{WDS}$) pulses and in conjunction with the appropriate control signals. One Write Data line is provided for each Write Data bit in a tape character.

2.7.3.3.1 $\overline{WDS}$ – Write Data Strobe. This is a clock signal which provides the necessary timing for the selected Tape Unit to copy the Write Data ($\overline{WDP}$ and $\overline{WD0}$ through $\overline{WD7}$). The Write Data levels must be static during $\overline{WDS}$. The positive-going transition (trailing edge) of the $\overline{WDS}$ pulse is used to clock the Write flip-flops in the Tape Unit. The clock rate is at the character rate for NRZI.

2.7.3.3.2 $\overline{WDP}$, $\overline{WD0}$ Through $\overline{WD7}$ – Write Data. $\overline{WDP}$ is the odd parity bit, $\overline{WD0}$ is the most significant bit in 9-track format, $\overline{WD2}$ is the most significant bit in 7-track format, and $\overline{WD7}$ is the least significant bit in both 7-track and 9-track formats. $\overline{WD0}$ and $\overline{WD1}$ are not used in 7-track format. These Write Data signals are presented to the selected Tape Unit along with the $\overline{WDS}$ clock strobe pulse. The Write Data is presented in logic-level form wherein Low = logic 1 and High = logic 0.

2.7.4 TAPE UNIT-TO-FORMATTER INTERFACE

Tape Unit-to-Formatter I/O cable interface pin assignments are also shown in Figure 2-4. Terms under bars are low (0V) when active, terms without bars are high (+5V) when active. There are up to 21 signal lines from the Tape Unit to the Formatter, which are grouped into two functional categories:

A. Tape Unit status information.
B. Read Data bits transfer.

2.7.4.1 Status

Eleven lines (ref. paragraphs 2.7.4.1.1 through 2.7.4.1.11) to the Formatter indicate the status of the Tape Unit.

2.7.4.1.1 $\overline{\text{RDY}}$ – Ready. A level which is low only when the Tape Unit meets the following conditions:

A. Initial load or rewind to load point (BOT) sequence has been completed.
B. Tape Unit is not rewinding.
C. On Line ($\overline{\text{ONL}}$) status signal is low.

NOTE

A Tape Unit will go NOT READY for approximately 0.5-second after reversing into Load Point, and does not go READY until approximately 0.5-second after termination of a Rewind.

2.7.4.1.2 $\overline{\text{ONL}}$ – On Line. A level which when low, indicates the selected Tape Unit is On Line and under remote control.

2.7.4.1.3 $\overline{\text{RWD}}$ – Rewind. A level which is low while the selected Tape Unit is rewinding. The level remains low until the Tape Unit completes the return-to-load-point sequence. The Tape Unit becomes Ready approximately 0.5-second after the RWD signal terminates.

2.7.4.1.4 $\overline{\text{FPT}}$ – File Protect. A low level on this line indicates no Write Enable ring is installed on the supply (file) reel of the selected Tape Unit.

2.7.4.1.5 $\overline{\text{LDP}}$ – Load Point. A level which is low when the Beginning of Tape (BOT) reflector on the tape in the selected Tape Unit is under the photo sensor, and the initial load or rewind sequence is completed.

NOTE

Load Point is the same as BOT.

2.7.4.1.6 $\overline{\text{EOT}}$ – End of Tape. A low level on this line indicates the selected Tape Unit is sensing the reflective marker at the end of the tape. This signal is not static and neither the positive-going nor negative-going transition is clean.

2.7.4.1.7 $\overline{\text{NRZ}}$/PE – Non Return to Zero/Phase Encoded. A level which indicates the type of Tape Unit selected: low is NRZ, high is PE.

2.7.4.1.8 $\overline{\text{SINGLE}}$/DUAL – Head Stack. A level which indicates the type of head in the selected Tape Unit: low is single-stack (Read/Write), high is dual-stack (Read-After-Write).

2.7.4.1.9 $\overline{\text{LOW}}$/HIGH – Tape Motion Speed. A level which indicates speed of selected Tape Unit: low is low-speed Tape Unit; high is high-speed Tape Unit.

2.7.4.1.10 $\overline{\text{7 TRK}}$/9 TRK – Tape Unit Tracks. A level which indicates the number of tracks in the selected Tape Unit: low is 7-track; high is 9-track.

2.7.4.1.11 $\overline{\text{DDI}}$ – Data Density Indicator. A level which indicates the selected data density in the selected Tape Unit: low is high density; high is low density.

2.7.4.2 Read Data

Read Data signals ($\overline{\text{RDP}}$ and $\overline{\text{RD0}}$ through $\overline{\text{RD7}}$) from the selected Tape Unit are sent to the Formatter along with timing signals of the Read Data Strobe ($\overline{\text{RDS}}$) pulses, and in conjunction with the appropriate control signals. One Read Data line is provided for each Read Data bit in a tape character.

2.7.4.2.1 $\overline{\text{RDS}}$ – Read Data Strobe. This is a clock signal with a negative-going pulse which indicates the Read Data bit being processed is valid. During a Read operation, an $\overline{\text{RDS}}$ pulse must accompany each valid data bit. $\overline{\text{RDS}}$ provides the necessary timing for the Read Data to be read. The Read Data levels must be static during $\overline{\text{RDS}}$. The positive-going transition (trailing edge) of the $\overline{\text{RDS}}$ pulse is used to clock the Read flip-flops in the Formatter.

2.7.4.2.2 $\overline{\text{RDP}}$, $\overline{\text{RD0}}$ Through $\overline{\text{RD7}}$ – Read Data. $\overline{\text{RDP}}$ is the odd parity bit, $\overline{\text{RD0}}$ is the most significant bit in 9-track format, $\overline{\text{RD2}}$ is the most significant bit in 7-track format, and $\overline{\text{RD7}}$ is the least significant bit in both 7-track and 9-track formats. $\overline{\text{RD0}}$ and $\overline{\text{RD1}}$ are not used in 7-track format. When presented to the Formatter, each Read Data bit signal is accompanied by an $\overline{\text{RDS}}$ pulse. The Read Data is presented in logic-level form: low is logic 1; high is logic 0.

2.7.5 CONTROLLER-TO-FORMATTER INTERFACE

Table 2-2 lists the Controller-to-Formatter I/O cable interface pin assignments. There are 26 signal lines from the Controller to the Formatter, which are grouped into five functional categories:

A. Addressing
B. Commands
C. Write Control
D. Modes
E. Write Data

The Controller driver circuits to the Formatter should be capable of sinking 30 mA when at the low level. These drivers need not supply any current when at the high level, since resistor terminations to +5V are supplied within the Formatter. The drivers need not be open-collector types because no wired-OR function is used.

Terms under bars are low (0V) when active; terms without bars are high (+5V) when active. The following paragraphs define the Pertec I/O compatible signals from Controller-to-Formatter.

2.7.5.1 Addressing

All addressing is accomplished with three signal lines: FAD, TAD0, and TAD1.

2.7.5.1.1 $\overline{\text{FAD}}$ – Formatter Address. A level which allows the same line to be used for the selection of either of two Formatters. When low, Formatter 1 is addressed; when high, Formatter 0 is addressed. The level must remain static throughout the execution of any command. Each Formatter may be internally jumpered to provide indication to the Controller whether its address is 0 or 1.

2.7.5.1.2 TAD0, TAD1 – Tape Unit Select Address Lines. These levels, listed in Table 2-3, are decoded by the Formatter to select one of the four Tape Units. The levels must remain static throughout all operations except Rewind. A Tape Unit can be commanded to rewind and a different Tape Unit can be selected immediately.

TABLE 2-2. Formatter/Controller I/O Cable Interface

J103 Pins	(Input) Controller to Formatter		J103 Pins	(Output) Formatter to Controller	
1	FAD		50	FMK	
2	TAD 0	Addressing	48	HER	
5	TAD 1		49	CER	
			56	FPT	
24	OFL		59	LDP	
7	REV/FWD		53	RDY	
23	REW		54	ONL	
8	WRT/READ	Commands	55	RWD	Status
11	WFM		60	EOT	
13	ERASE		65	7 TRK	
12	EDIT (not used)		66	SGL	
			67	SPD	
6	GO –	Command Clock	62	NRZ	
26	FEN –	Formatter Enable	43	FBY	
			44	DBY	
19	PAR	Write Control	62	NRZ	
25	LWD		47	CCG/IDENT *	
14	THR1		72	RP	
17	THR2	Modes	73	R0	
18	DEN		74	R1	
			77	R2	Read
30	WP (not used)		78	R3	Data
31	W0		79	R4	
32	W1		80	R5	
35	W2	Write	83	R6	
36	W3	Data	84	R7	
37	W4				
38	W5		71	RSTR –	Read Clock
41	W6				
42	W7		68	WSTR –	Write Clock
3, 4, 9, 10, 15, 16, 21, 22, 27, 28, 33, 34, 39, 40, 45, 46, 51, 52, 57, 58, 64, 69, 70, 75, 76, 81, 82, 96, 98, 100 – Signal GND					

* CCG/IDENT is a time shared line. For PE units, the signal is known as IDENTS. For NRZI units, the signal is known as CCG.

TABLE 2-3. Tape Unit Select Address Line Levels

TAD0 Level	TAD1 Level	Tape Unit Selected
High	High	0
High	Low	1
Low	High	2
Low	Low	3

2.7.5.2 Commands

All commands are clocked into the Formatter by the GO command clock pulse. The command signals must be static for a minimum of 500 nanoseconds before and after the command clock pulse.

2.7.5.2.1 OFL – Offline. A low-true pulse on this line places selected Tape Unit in Offline mode.

2.7.5.2.2 REV/FWD – Reverse/Forward. A low level on this line selects reverse mode. Conversely, a high level selects forward mode.

2.7.5.2.3 REW – Rewind. A low true pulse on this line selects a Rewind operation on the selected Tape Unit.

2.7.5.2.4 WRT/READ – Write/Read. A low level on this line selects Write mode. Conversely, a high level selects Read mode.

2.7.5.2.5 WFM – Write File Mark. A low level on this line, when WRT/READ line is low, causes a file mark to be written by the selected Tape Unit.

2.7.5.2.6 ERASE – Erase. A low true level on the ERASE, WRT/READ, and WFM lines conditions the Formatter to execute a fixed-length erase of approximately 3 inches of tape. No variable length erase function is provided.

2.7.5.2.7 GO – Command Clock. All commands, except Rewind and Off Line are clocked into the Formatter on the trailing edge of the clock pulse.

2.7.5.2.8 FEN – Formatter Enable. A high true pulse or level on this line resets all Formatter operations.

2.7.5.3 Write Control

The Write Control lines control transfer of data during Write mode.

2.7.5.3.1 PAR – Parity. This line is used only for 7-track NRZI units. A low true level on this line enables generation of even parity in Write mode.

2.7.5.3.2 LWD – Last Word. When a low true level is generated on this line at the same time the last character of a record is transmitted, it indicates no further Write data transfers are required.

2.7.5.4 Modes

The Mode functions are clocked into the Formatter with a GO command.

2.7.5.4.1 THR1, THR2 – Read Threshold Levels. For single-gap Tape Units, a low true level on THR1 selects a high read threshold level. A low true level on THR2 selects a low read threshold level, to enable detection of low-amplitude tape data.

2.7.5.4.2 DEN – Density. When the Formatter is used as part of a PE/NRZI system, this line provides selection of either the PE or NRZI Formatters. A low true level selects the NRZI Formatter. Conversely, a high level selects the PE Formatter. When used for 7-track tape systems, a low true level selects the lower of two possible bit densities for Write or Read operations.

2.7.5.5 Write Data

The Write data is transferred from the Controller to the Formatter over 8 lines, W0 through W7. The WP (Write Parity) line is not used.

2.7.5.5.1 W0 through W7 – Write Data. W0 through W7 comprise the low true data input lines. W0 is the most significant bit; W7 is the least significant bit.

2.7.6 FORMATTER-TO-CONTROLLER INTERFACE

There are 28 signal lines from the Formatter to the Controller (ref. table 2-2) which are grouped into four categories:

A. Status
B. Read Data
C. Read Clock
D. Write Clock

2.7.6.1 Status

The Status lines are supplied to the Controller as indications of the Formatter or Tape Unit operating functions.

2.7.6.1.1 FMK – File Mark. A low true 1-microsecond pulse on this line indicates a file mark has been detected.

2.7.6.1.2 HER – Hard (Non-correctable) Error. A low true level on this line indicates a non-correctable error has been detected.

2.7.6.1.3 CER – Corrected Error. A low true 1-microsecond pulse on this line indicates a correctable error has been detected. It is not used in the NRZI Formatter.

2.7.6.1.4 FPT – File Protect. A low true level on this line indicates the Tape Unit is file protected, ie; that a Write operation cannot be performed unless a Write Enable ring is installed on the file reel or cartridge.

2.7.6.1.5 LDP – Load Point. A low true level on this line indicates the Tape Unit is at the load point (BOT).

2.7.6.1.6 RDY – Ready. A low true level on this line indicates the Tape Unit is ready to accept Controller commands.

2.7.6.1.7 ONL – On Line. A low true level on this line indicates the selected Tape Unit is On Line.

2.7.6.1.8 RWD – Rewind. A low true level on this line indicates the selected Tape Unit is performing a Rewind operation.

2.7.6.1.9 EOT – End of Tape. A low true level on this line indicates the selected Tape Unit has reached the End of Tape (EOT) marker.

2.7.6.1.10 7 TRK – 7 Track. A low true level on this line indicates selection of a 7-track Tape Unit. Conversely, a high true level on this line indicates selection of a 9-track Tape Unit.

2.7.6.1.11 SGL – Single. A low true level on this line indicates the selected Tape Unit has a single-gap head. Conversely, a high level on this line indicates the selected Tape Unit has a dual-gap head.

2.7.6.1.12 SPD – Speed. This line is used in systems which have Tape Units of different speeds. A low true level on this line indicates the selected Tape Unit is operating in the low-speed mode. Conversely, a high level on this line indicates the selected Tape Unit is operating in the high-speed mode.

2.7.6.1.13 FBY – Formatter Busy. A low true level on this line indicates the Formatter is performing a functional operation.

2.7.6.1.14 DBY – Data Busy. A low true level on this line indicates a Write or Read mode operation is in progress.

2.7.6.1.15 NRZ – Non-Return to Zero. A high level on this line indicates the Formatter is in the PE mode of operation.

2.7.6.1.16 CCG/IDENTS – Identification Burst. A low true pulse on this line indicates the Formatter has detected the NRZI check characters on the tape.

2.7.6.2 Read Data

Nine Read Data lines transfer parallel Read data to the Controller. They are clocked by the Read clock which generates the Read Strobe (RSTR) pulse.

2.7.6.2.1 RP, R0 through R7 – Read Data. The Read data is transmitted in a low-true format. RP is the parity character. R0 is the most significant bit; R7 is the least significant bit.

2.7.6.3 RSTR – Read Strobe. A Read Strobe (clock) pulse is generated for each Read character transmitted. Each clock pulse has a duration of approximately one microsecond.

2.7.6.4 WSTR – Write Strobe. A Write Strobe (clock) pulse is generated for each Write character transmitted. The first character must precede the first clock pulse, with each subsequent character on-line within one-half of a character period after the trailing edge of each clock pulse.

SECTION 3

OPERATION

3.1 GENERAL

In this section, physical operation of the WANGCO Model 511 NRZI Formatter is described, pre-operational checkouts are defined, and front panel switches and indicators are identified.

3.2 CHECKS BEFORE OPERATION

After the Formatter has been installed, the following checks should be made before operation is begun:

A. Verify that I/O cables are properly located and firmly seated to ensure correct interface connections.

B. Verify that the two fuses, accessible from the rear panel, are of the voltage and amperage rating marked on the Formatter.

C. Before applying AC line power, verify that line voltage corresponds to the voltage marked on the Formatter (ref. figure 2-1).

3.3 OPERATION

Formatter operation is simple. Only initial control switch settings on the Operator Control Panel (OCP) need be made. With initial control settings established, the selected Formatter automatically performs all commanded operations. No adjustments are required. Controls and indicators are shown in Figure 3-1.

3.3.1 POWER SWITCH/INDICATOR

A push-on/push-off switch/indicator. AC power is applied, or removed, by pressing. Internal indicator is lit when power is on. No warm-up time is required for the Formatter.

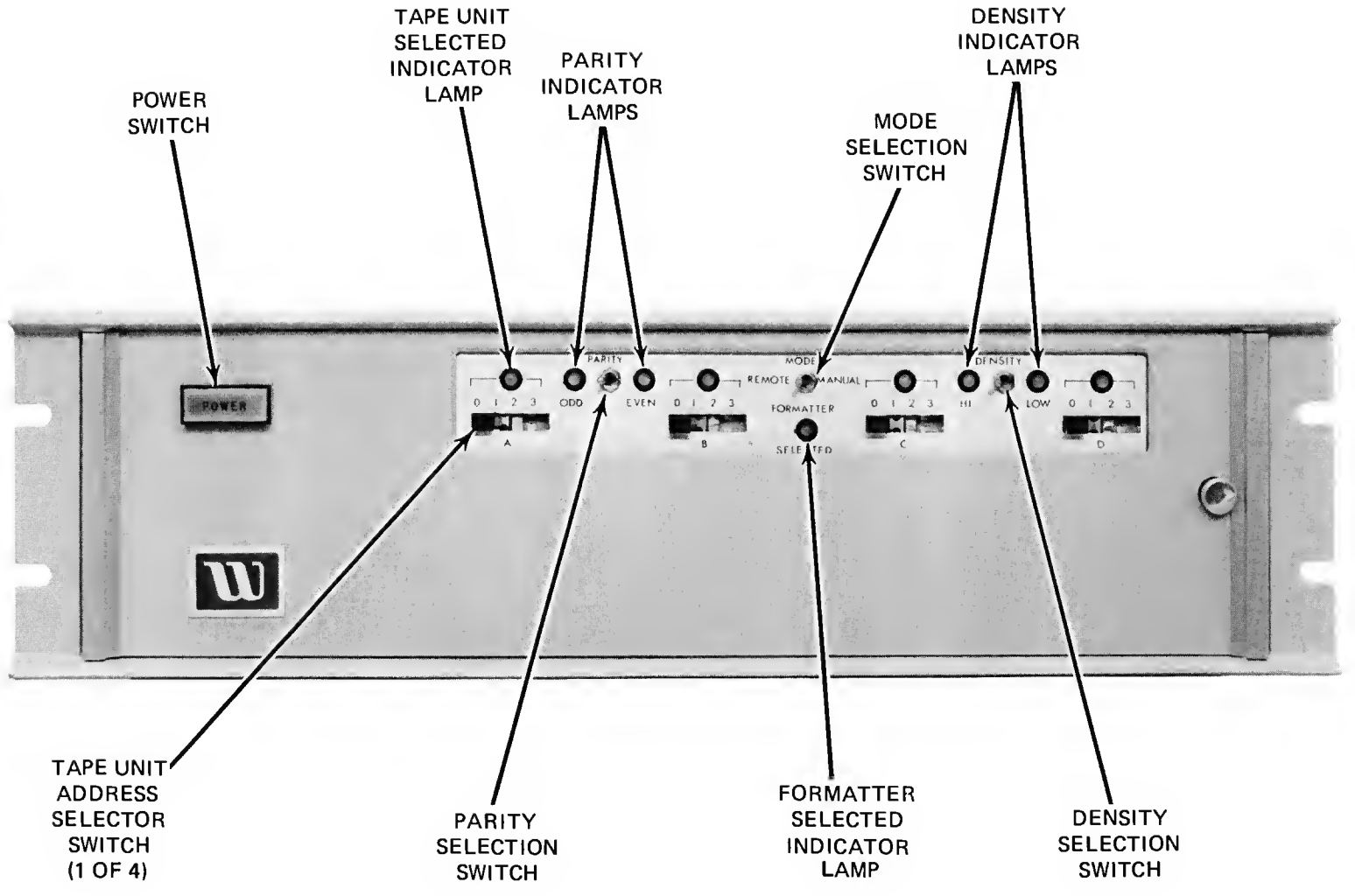


Figure 3-1. Front View of Formatter Operator Control Panel

3.3.2 TAPE UNIT ADDRESS SELECTOR SWITCHES

Four 4-position, detented slide switches (A, B, C, and D), each with selectable positions 0, 1, 2, or 3. If multiple Tape Units are used (daisy-chained), each Tape Unit (0, 1, 2, or 3) must be assigned a unique address by using these switches; e.g., A = 0, B = 1, C = 2, D = 3. Tape Units assigned the same address are simultaneously selected.

3.3.3 TAPE UNIT SELECTED INDICATOR LAMPS

One of these indicator lamps is located above each Tape Unit Address Selector Switch. When a Tape Unit is selected, its corresponding lamp is lit.

3.3.4 FORMATTER SELECTED INDICATOR LAMP

This indicator lamp is lit when the Formatter is selected.

3.3.5 MODE REMOTE/MANUAL SELECTOR SWITCH

A 2-position toggle switch. Its position determines whether control of parity and density is manually selected by OCP switches on the front panel or remotely controlled from the Controller.

NOTE

Only 7-track Tape Units are affected by the position of the MODE, PARITY, and/or DENSITY select switches; 9-track Tape Units are always odd parity with 800 BPI density.

3.3.6 PARITY ODD/EVEN SELECTOR SWITCH

A 2-position toggle switch. Allows selection of either odd or even parity data to be written or checked by the Formatter when 7-track Units are selected (ref. paragraph 3.3.5 and associated note). Parity selected must be the same as that of the selected 7-track Tape Unit. This switch has no effect when 9-track Tape Units are selected, or when the MODE switch is in the REMOTE position.

3.3.7 PARITY ODD/EVEN INDICATOR LAMPS

The lamp corresponding to the PARITY switch position is lit, regardless of the MODE switch position or Tape Unit selected, to indicate the parity configuration of the Formatter. The illuminated lamp is significant only when the MODE switch is in the MANUAL position and a 7-track Tape Unit is selected (ref. paragraph 3.3.5 and associated note).

3.3.8 DENSITY HI/LOW SELECTOR SWITCH

A 2-position toggle switch. Allows selection of either of two possible densities for any selected 7-track Tape Unit. Density selection, however, is relative and is established by density-jumper positions selected, if used, for each Tape Unit (refer to Section 4 for additional information on this option). This switch has no effect when 9-track Tape Units are selected, or when the MODE switch is in the REMOTE position (ref. paragraph 3.3.5 and associated note).

3.3.9 DENSITY HI/LOW INDICATOR LAMPS

The lamp corresponding to the DENSITY switch position is lit, regardless of the MODE switch position or Tape Unit selected, to indicate the density configuration of the Formatter. The illuminated lamp is significant only when the MODE switch is in the MANUAL position and a 7-track Tape Unit is selected (ref. paragraph 3.3.5 and associated note).

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section contains theory of operation of the WANGCO Model 511 NRZI Tape Unit Formatter. The Formatter can accommodate as many as four Tape Units simultaneously. For the multiple Tape Unit configuration, all input/output signal lines are daisy chained, while a single select line is wired to each individual Tape Unit. Only the selected Tape Unit responds to the Formatter commands. The Formatter performs three basic functions:

A. Control
B. Write
C. Read

The information in this section is divided into two major topics. A discussion on a block diagram level is presented first to provide an overall functional description and to illustrate the relationship between the Formatter, the Tape Units, and the Controller. A discussion of the command execution, illustrated by timing diagrams, describes operation of the Formatter circuitry during execution of computer-originated instruction.

4.1.1 CONTROL

The Formatter provides control over the selected Tape Unit including all timing necessary to automatically perform all commands. Upon completion of the commanded operation, status is provided so that the Computer can ascertain whether the operation was performed correctly.

4.1.2 WRITE

The Formatter performs all the Write functions for erasing tape, writing a file mark, or writing a data record. A 3-inch (7.62cm) gap is automatically erased before the first record when starting from beginning of tape (BOT). The correct timing delays for erasing the inter-record gap (IRG) is provided, and the File-Mark code is developed by the Formatter.

4.1.3 READ

The Formatter also reduces Read operations to a minimum by performing all parity checks and automatically positioning the Inter-record gap (IRG) under the heads.

4.2 BLOCK DIAGRAM DISCUSSION

Figure 4-1, a simplified block diagram, illustrates the various functions performed by the standard 7-track, 9-track NRZI Formatter and shows the relationship between the Formatter, the Tape Units, and the Controller. The hexagon-enclosed numbers refer to the Logic Diagram Number on which the indicated function is drawn in detail. This number is located in the lower right-hand corner of the detailed logic drawings.

4.2.1 EMULATOR INTERFACE LOGIC (Dwg. 202234)

The Emulator Interface provides a compatible interface between a Controller that uses a Pertec I/O format and the standard WANGCO I/O format. This allows replacement of a standard Pertec Formatter with a WANGCO Formatter, and retains the use of the existing Controller.

Because of the Emulator design, the following functions that are available with the Pertec Formatter are not available with the modified WANGCO Formatter:

A. No variable Erase function (only fixed-length Erase function).
B. No Edit function.
C. No external Write parity generation option. Odd parity for the Write function is generated by the Formatter.
D. No transfer of CRC or LRC characters.

4.2.1.1 Input Conversion

The following paragraphs describe the conversion of the predominately low true commands from a Controller that uses the Pertec signal format to the input level requirements of the WANGCO circuitry. In the following paragraphs, the input signal nomenclature follows the standard Pertec format.

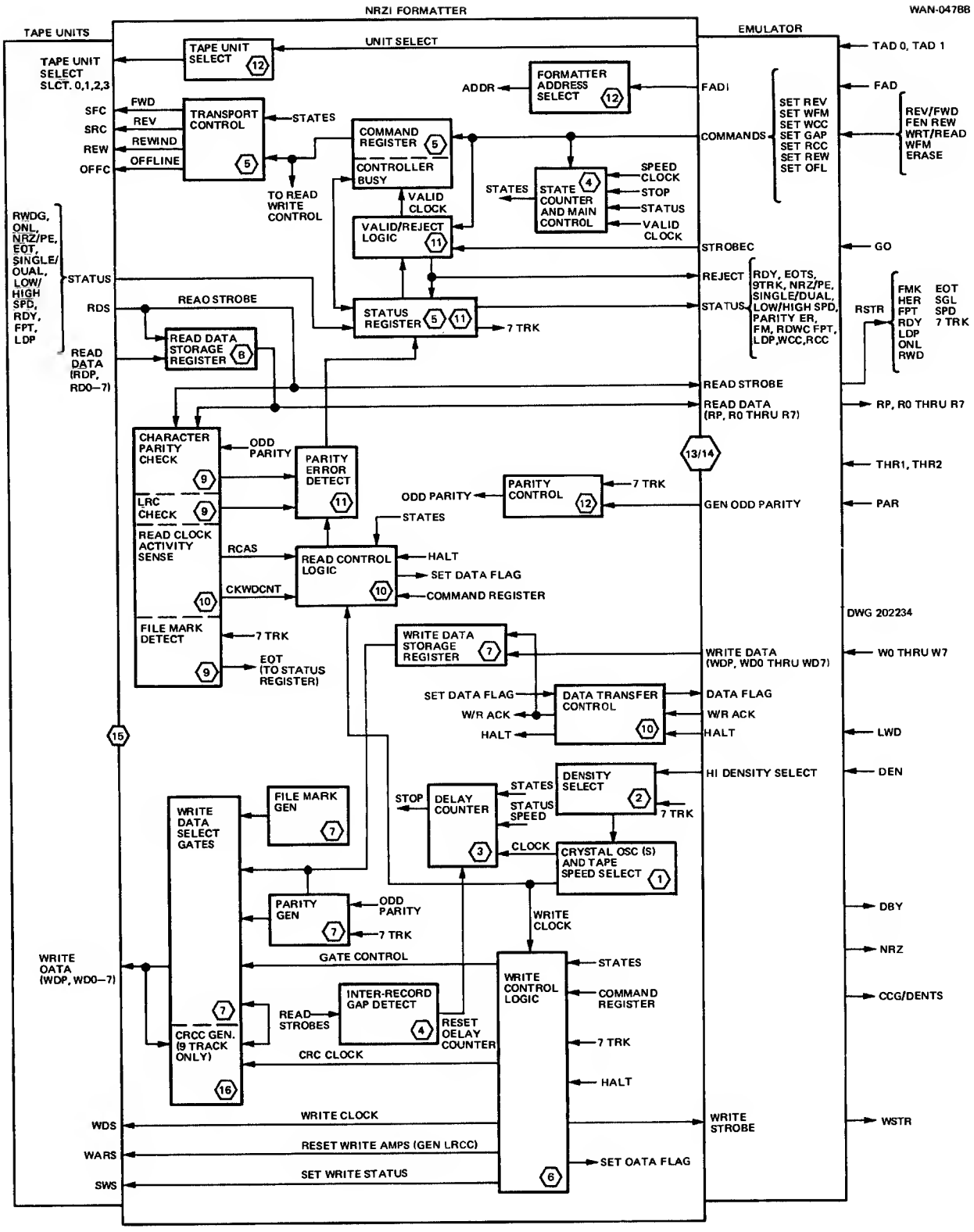


Figure 4-1. NRZI Formatter Block Diagram

4.2.1.1.1 FAD Command. This input command is terminated, buffered, and supplied to the Formatter circuitry (without inversion) as the FAD signal.

4.2.1.1.2 TAD0, TAD1, REV/FEW, FEN, REW Commands. These input commands are terminated, inverted and supplied to the Formatter circuitry as WANGCO signals S2, S1, SET REV, EXT RESET, and SET REW, respectively.

4.2.1.1.3 WRT/READ, WFM, ERASE Commands. These input commands are used to generate four WANGCO signal commands; SET RCC, SET WCC, SET WFM, and SET GAP. Table 4-1 lists a truth table which illustrates the command-level requirements for generation of the WANGCO signals.

TABLE 4-1. Input Command Truth Table

WANGCO Signals (high)	WRT/READ	WFM	ERASE
SET RCC	high	high	high
SET WCC	low	high	high
SET WFM	low	low	high
SET GAP	low	low	low (fixed-length erasure)

4.2.1.1.4 GO Line. A low true pulse level on this line generates the WANGCO command clock signal, STROBEC. Because the rewind (REW) command or the Off-Line (OFL) command from the Pertec interface is not accompanied by a GO pulse, a monostable (one-shot) circuit is used to generate the required STROBEC command pulse. If a REW or OFL command is issued, the one-shot provides a 300-nanosecond STROBEC pulse to Formatter circuitry.

4.2.1.1.5 THR1, THR2 Lines. The pulse levels on each of these lines are clocked into a latch flip-flop (F-F) by a STROBEC pulse and supplies the $\overline{\text{THR1}}$ and $\overline{\text{THR2}}$ levels to Formatter circuitry.

4.2.1.1.6 DEN Line. The pulse level on the Density line is clocked into a latch F-F by a STROBEC pulse and supplies the $\overline{\text{HI DENSITY}}$ mode line to Formatter circuitry.

4.2.1.1.7 DATA FLAG and W/R ACK Signals. As shown in Figure 4-2, $\overline{\text{DATA FLAG}}$ from the Formatter is inverted and held one microsecond, then gated with DATA FLAG to generate the $\overline{\text{W/R ACK}}$ signal. $\overline{\text{W/R ACK}}$ internally resets the Formatter $\overline{\text{DATA FLAG}}$ signal and causes F-F A to be reset. This sequence continues for each transferred data character until Last Word (LWD) is received from the Pertec interface. A low level on the LWD line enables F-F B, which supplies the high true HALT command to the Formatter. F-F B is reset by either a command clock (STROBEC) pulse or a low true level on the RCC status line. This indicates the Formatter is in the Read mode.

4.2.1.1.8 PAR Line. The pulse level on the Parity line is clocked into a latch F-F by a STROBEC pulse and supplies the GEN ODD PARITY signal to Formatter circuitry.

4.2.1.1.9 W0 through W7. The low true signals from the Controller are terminated, buffered, and supplied to the Formatter as low true Write signals B0 through B7.

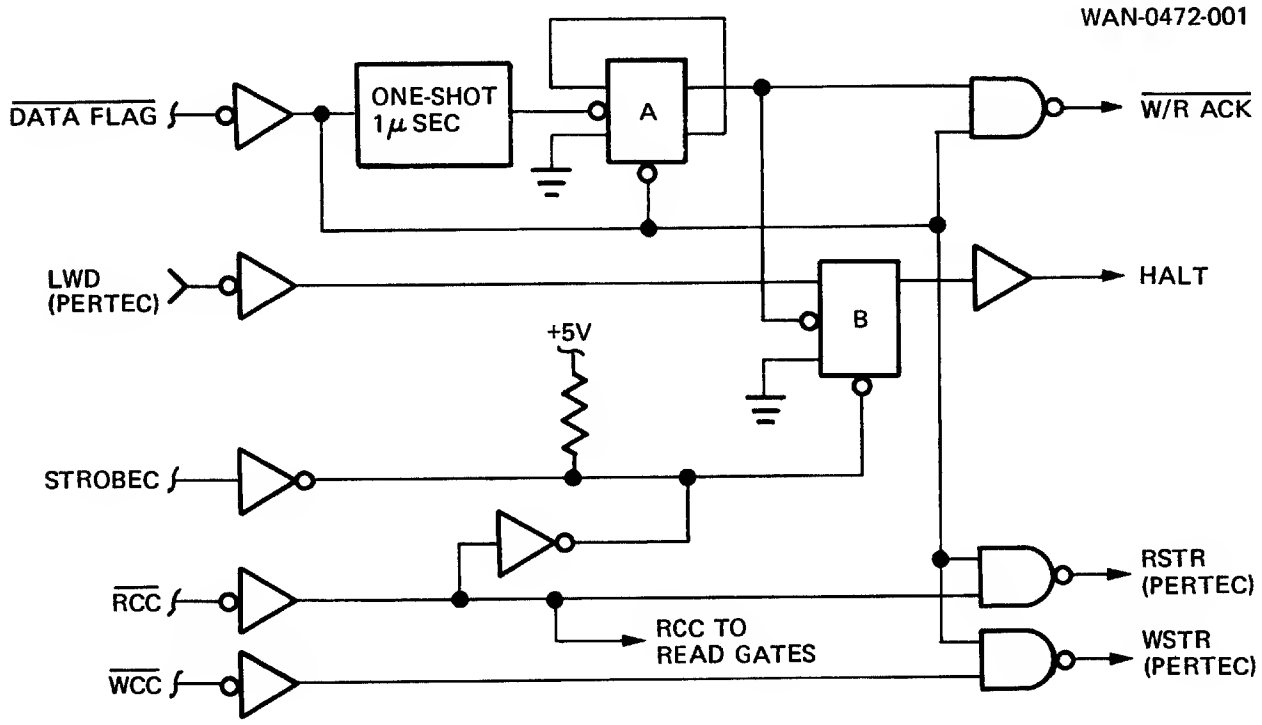


Figure 4-2. HALT and W/R ACK Command Logic

4.2.1.2 Output Conversion

The following paragraphs describe the conversion of the low true Formatter output signals to the levels required by a Controller that uses Pertec signal format. In the following paragraphs, the output signal nomenclature follows the standard Pertec format.

4.2.1.2.1 WSTR, RSTR. A low true Read Strobe (RSTR) signal is generated by gating the Formatter Read status line (RCC) with DATA FLAG. Similarly, Write Strobe (WSTR) is generated by gating the Formatter Write status line (WCC) with DATA FLAG (ref. figure 4-2).

4.2.1.2.2 FMK, CER. As shown in Emulator logic Dwg. 202234, both the File Mark (FMK) and Correctable Error (CER) status signals are generated by inverting the corresponding Formatter signal ($\overline{FM}$ and $\overline{CERS}$, respectively), to trigger a one-shot, which generates a 1-microsecond pulse. This pulse is then inverted and supplied as a low true status-output signal to the Controller.

NOTE

CERS is not available from the NRZI Formatter; therefore, CER is always false (high) from the Emulator.

4.2.1.2.3 HER. The noncorrectable Hard Error (HER) is generated by inverting the Formatter $\overline{PARITYER}$ signal and gating it with CERS to provide a low true output signal to the Controller.

4.2.1.2.4 FPT, LDP, RDY, ONL, RWD, EOT, 7 TRK, SGL, SPD. These status signals are simply the buffered, low true Formatter status-output signals; except for 7-TRK, which is the inverted $\overline{9\ TRK}$ Formatter output signal.

4.2.1.2.5 FBY, DBY, NRZ. These Read control signals are simply the buffered, low true Formatter output signals.

4.2.1.2.6 CCG/IDENT. For NRZI units, this line is known as CCG. A low true pulse on this line indicates the NRZI check characters have been detected by the Formatter. The $\overline{RCAS}$ and $\overline{NRZ}$/PE signals are inverted and NAND'ed to set F-F U9. F-F U9 is reset by gating $\overline{NRZ}$/PE and $\overline{DBY}$; thus, the resultant output signal is $\overline{RCAS \cdot DBY}$.

4.2.1.2.7 RP, R0 through R7. The low true Read signals from the Formatter are inverted and gated with the Read Status signal (RCC) to supply the low true Read lines to the Controller. Jumper selection is provided to make the Read signals available only in the Read mode (jumper E1–E2) or in both modes (jumper E2–E3).

4.2.2 COMMAND REGISTER AND VALID/REJECT LOGIC ⟨5⟩⟨11⟩

When a command is output from the Computer, the command and a strobe pulse are delivered from the Controller to the Valid/Reject logic of the Formatter. If the command is acceptable, a valid clock is generated to enable the command to be loaded into the Command Register. If the command is not valid, a reject pulse is returned to the Controller. Each valid clock initiates a system reset (SRS) pulse which is used to reset the Formatter to initial conditions.

4.2.2.1 Controller Busy. The valid clock also sets the Controller Busy (CBUSY) F-F. Normally, the CBUSY F-F is used by the Controller to signal termination of all commands. The Transport Control logic resets the CBUSY F-F after all tape motion has ceased for the commanded function. If On-the-Fly writing or reading is desired, the Data Busy status must be used by the Computer to initiate the next command as soon as Data Busy terminates.

4.2.3 TRANSPORT CONTROL LOGIC ⟨5⟩

The Transport Control logic develops the FWD, REV, REWIND and OFFLINE commands to the selected Tape Unit under control of the Command Register and the State Counter.

4.2.4 FORMATTER ADDRESS SELECT LOGIC ⟨12⟩

The Formatter Address Select logic allows a Formatter to be assigned the number zero or one so that two Formatters can be daisy-chain connected to one Controller to provide control for up to eight Tape Units or a mixture of NRZI and 1600 BPI Phase-Encoded Tape Units.

4.2.5 TAPE UNIT SELECT LOGIC ⟨12⟩

The Tape Unit Select switches allow the operator to assign unit numbers 0, 1, 2, or 3 to any of the four Tape Units. This allows physical Tape Units to be switched without requiring changes to the Computer program. Indicator lamps on the Formatter provide visual indication of which Tape Unit is selected.

4.2.6 STATE COUNTER AND MAIN CONTROL LOGIC 4

The State Counter divides the major operations (such as Write and Read) into successive states (suboperations) that are sequentially stepped through to perform the complete major operation. These states are shown in Table 4-2.

TABLE 4-2. State Count Versus Function

State Count	Function
0	Rest
1	Predelay, not BOT and not 3-inch (7.62cm) gap.
2	Predelay, BOT or 3-inch (7.62cm) gap.
3	Write or Read execution
4	Postdelay
5	Forward Motion Halt time out
6	Reverse Motion Halt time out
7	Rewind or Clear execution

4.2.6.1 Delay and Time Out States. The Delay and Time Out states all use the Delay Counter to determine when the state count should terminate and when the next state count can be entered. These delay-count times very depending on the following factors:

A. Tape speed
B. Single- or dual-stack head
C. Edit or normal mode
D. Reverse or forward motion
E. Seven- or nine-track Tape Unit selected

The pre- and post-delays are used to erase the inter-record gaps (IRG) and to halt the tape under the head in the correct position in the IRG when reading.

4.2.6.2 State Descriptions. Brief descriptions of the eight states (0 through 7) are provided below.

A. State 0 (the "Rest" state) is the state the Formatter enters after completing an operation.
B. State 1 (Predelay) is used to wait for the Tape Unit to get up to speed and to erase part of the IRG when writing. State 1 is used for Predelay when not starting from BOT or when not erasing a 3-inch (7.62cm) gap.

C. State 2 (Predelay) is similar to State 1 except a longer delay is implemented to handle the 3-inch (7.62cm) gap erased automatically at BOT and for the erase 3-inch (7.62cm) gap command.

D. State 3 (Write or Read Execution) is the State during which the record is written or read. When reading, State 3 is terminated when no more Read Strobes occur. This indicates the IRG has been reached.

E. IRG detection is also used to terminate State 3 for Write operations when using a dual-stack Read-After-Write Tape Unit. This allows the written record to be checked for correct parity. For single-stack Write operations, State 3 is terminated as soon as the LRC character is written at the end of the record.

F. State 4 (Postdelay) is used when reading to halt the tape under the head in the correct position in the IRG. When writing, State 4 Postdelay erases a portion of the IRG.

G. State 5 (forward motion halt time out) retains memory of the forward direction of motion during the time interval after the Tape Unit has been commanded to stop until the Tape Unit actually stops. This delays termination of the CBUSY signal until the Tape Unit has completely halted the tape in the IRG. The DBY status terminates when State 5 or 6 is entered so that successive Write or Read operations may be executed On-the-Fly without stopping in the IRGs.

H. State 6 (reverse motion halt time out) is similar to State 5, except for reverse motion commands.

I. When performing On-the-Fly operations, successive commands issued after DBY terminates but before CBUSY terminates must be of the same type. A Read command cannot follow a Write command and a forward motion command cannot follow a reverse motion command (or vice versa). There is, of course, no such restriction if the commands are not issued until after CBUSY terminates.

J. State 7 (Rewind or Clear) is entered upon issuance of a Rewind or Clear command by the Computer. The State is terminated when the Tape Unit finishes rewinding.

4.2.7 STATUS REGISTER LOGIC ⟨5⟩⟨11⟩

The Status Register stores both Tape Unit and Formatter status so that the Computer can inspect the results of an operation after the operation is completed to find out whether the operation was correctly completed or whether some other action needs to be taken. The status of the selected Tape Unit and the Formatter are available for access by the Computer at any time.

4.2.8 PARITY CONTROL LOGIC ⟨12⟩

The Parity Control logic provides manual or program control over selection of odd or even parity for 7-track Tape Units. Odd parity is automatically selected for 9-track Tape Units. The output (odd parity) is used by the Parity Generator and check logic.

4.2.9 PARITY ERROR DETECT LOGIC ⟨11⟩

The Parity Error Detect logic searches for one or more parity errors in each tape record. Any detected errors causes the Parity Error Status bit to be set. The Read Control logic uses the Read Clock Activity Sense (RCAS) logic output to enable the Parity Error Detect logic to inspect the output of the Character Parity Check logic only during the data portion of a record; since CRCC 9-track and LRCC 7-track can exhibit either odd or even parity. The output of the LRC Check logic is inspected only after the entire record (including CRCC and LRCC) has been read.

4.2.10 CHARACTER PARITY CHECK LOGIC ⟨9⟩

The Character Parity Check logic checks each character read from tape for either odd or even parity under control of the Parity Control logic.

4.2.11 LRC CHECK LOGIC ⟨9⟩

The Longitudinal Redundancy Character Check logic checks for an even number of 1's for each individual track down the length of the record and includes the CRC and LRC characters.

4.2.12 READ DATA STORAGE REGISTER LOGIC ⟨8⟩

The Read Data Storage Register stores each tape character at the leading edge of the Read Strobe in such a manner that the Read Data is static to the Controller interface throughout the entire period until the leading edge of the next Read Strobe occurs. This obviates the requirement for a storage register in the Controller which would otherwise be required to retain the data for the maximum possible time after DATA FLAG is set to give the Computer the maximum amount of time to accomplish the data transfer. The outputs of the Read Data Storage Register are routed to the rest of the logic where Read data is utilized in the Formatter.

4.2.13 READ CLOCK ACTIVITY SENSE LOGIC (10)

The Read Clock Activity Sense logic is used to separate the data portion of each record from the CRC and/or LRC characters in the Forward direction; thus, the Set Data Flag (in the Read Control logic) is allowed to operate only for the data portion of the record which strips off the CRC and/or LRC characters.

4.2.13.1 Check Word Count. The Check Word Count (CKWDCNT) pulse occurs just after the last data character but before the CRC or LRC character's Read Strobe destroys the contents of the Read Data Storage Register. The CKWDCNT pulse is delivered to the Controller interface when an odd number of characters are read from tape while the Pack mode of operation is being used. The CKWDCNT pulse is also used on the Controller to determine if the expected number of characters was read from tape to create status bits which can inform the Computer that the record was too long, too short and/or contained an odd number of characters.

4.2.14 FILE MARK DETECT LOGIC (9)

The File Mark Detect logic checks for 7-track or 9-track file marks which depends on which type of Tape Unit is selected. The FM status is developed if a file mark is detected in either a forward or reverse direction.

4.2.15 READ CONTROL LOGIC (10)

The Read Control logic controls data transfer during State 3 until the IRG is detected. At this time, the Postdelay (State 4) or one of the Halt delays (State 5 or 6) is entered.

4.2.15.1 Set Data Flag Signal. The Set Data Flag signal is generated for each Read Strobe that occurs as long as RCAS indicates the data portion of the record is present and the Halt signal has not occurred.

4.2.15.2 IRG or Halt Signal. When the IRG is detected or when the Computer generates the Halt signal (to indicate it does not want any more data), no more Data Flag signals are generated even though there may be more data in the record.

4.2.15.3 Reading Backward. When reading backward, the CRC and/or LRC characters are not stripped from the data portion of the record, but are included as the first one or two characters read; therefore, these characters must be accounted for and stripped off by the program. The program accounts for these extra characters by setting the expected record length to two characters greater for 9-track and one character greater for 7-track. The program can strip off the extra characters by noting the length of the record and making one of the following responses:

A. For 9-track Tape Units: if the record was the expected two characters longer, then the first two characters are the LRC and CRC characters and may be discarded. If the record is not two characters longer, then the CRC character was all zeros (no Read Strobe occurs); thus, only the first character (LRC) needs to be discarded.

B. For 7-track Tape Units: If the record was the expected one character longer, the first character is the LRC character and may be discarded. If the record is not one character longer, then the LRC character must have been all zeros; thus, no character needs to be discarded.

4.2.15.4 Space Operations

The Read Control logic also controls the forward and reverse space operations. These operations are identical to reading forward or reverse, except the Data Flag is not set for data transfer requests. All parity checks are valid for spacing and reading operations, and for Read-After-Write operations when a dual-stack head is used on the selected Tape Unit. The following special Read modes may also be used:

A. Test Read
B. Read Threshold High
C. Read Threshold Extra Low

4.2.15.4.1 Test Read Mode. In the Test Read mode, the CRC and/or LRC characters are not separated from the data in the forward Read operation. This allows checking of the CRC and LRC generator logic by diagnostic programs.

4.2.15.4.2 Read Threshold High Mode. The Read Threshold High mode may be used with single-stack Read/Write Tape Units to enable a marginal parity check to be performed on each record immediately after it is written by backspacing over the record then spacing or reading forward over the record in the Read Threshold High mode, then checking for parity error status. This marginal check function is automatically performed by dual-stack Read-After-Write Tape Units since they automatically select the high threshold when in the Write mode so that Read-After-Write parity checks may be performed while writing.

4.2.15.4.3 Read Threshold Extra Low Mode. The Read Threshold Extra Low mode allows Tape Units equipped with this option to recover low-amplitude signals on tapes of poor quality.

4.2.16 WRITE DATA STORAGE REGISTER LOGIC ⟨7⟩

The Write Data Storage Register is provided so that no register is needed on the Controller to store output data from the Computer. The Data Transfer logic operates on a request/response basis via the Data Flag and Write/Read Acknowledge (W/R ACK) signals such that each character is requested a full write-clock period before it is needed, and the Computer can respond any time within this period with a W/R ACK strobe pulse to load the Write Data into the Write Storage Register.

4.2.17 PARITY GENERATOR LOGIC ⟨7⟩

The Parity Generator creates odd or even parity for each character presented from the Write Storage Register, then sends the parity bit to the Write Data Select Gates. The Parity Control logic determines whether odd or even parity is generated.

4.2.18 WRITE DATA SELECT GATES LOGIC ⟨7⟩

The Write Data Select Gates consist of three sets of gates which are enabled by the Write Control logic to gate the Write data (and parity bit), or the File Mark code, or the CRC Character onto the Write data bus to the Tape Units.

4.2.19 FILE MARK GENERATOR LOGIC ⟨7⟩

The File Mark Generator generates the appropriate file-mark code which depends on whether a normal 9-track file mark, a special 9-track file mark, or a 7-track file mark is to be written. The Write Control logic gates the file-mark code onto the Write data bus at the appropriate time and generates a Write Clock to write the file mark. The special 9-track file mark is an option that writes the 7-track file-mark code to provide compatibility with some models of computer hardware and software when writing in the unpack mode on a 9-track tape.

4.2.20 CRCC GENERATOR LOGIC ⟨16⟩

The Cyclic Redundancy Check Character (CRCC) Generator calculates the CRC character while writing each record (as each data character appears) on the Write data bus. At the end of the record (9-track Tape Unit only), the Write Control logic gates the CRCC onto the Write data bus and generates a Write Clock pulse to Write the CRC character. The LRC character is then written to finish the record. The CRCC may be all zeros and may exhibit odd or even parity.

4.2.21 WRITE CONTROL LOGIC ⟨6⟩

The Write Control logic operates during State 3 for Write, Erase and Write-File-Mark operations. The Write Control logic controls the Data Transfer logic for Write operations by developing the Set Data Flag pulse to request each character to be written until the Write operation is terminated by the Halt signal from the Controller.

4.2.21.1 Halt Signal. Upon receiving the Halt signal, the CRC and/or LRC character is automatically appended to the record, then part of the IRG is erased. If a single-stack (Read/Write) Tape Unit is selected, the Write Control logic triggers the State Counter to the State 4 postdelay after writing the LRC character at the end of the record. If a dual-stack (Read-After-Write) Tape Unit is selected, the Inter-Record Gap Detect logic is used to exit State 3 and enter State 4 (Postdelay). This allows all of the record to be Read-After-Write parity checked.

4.2.21.2 Data Rate. The data rate is developed from the Write Clock frequency generated by the Crystal Oscillators and Tape-Speed Select logic. The Write Control logic also sends the Write Most Significant Byte (WRMSB) signal to the Controller to enable the odd/even characters to be separated when unpacking a computer word into two sequential tape characters.

4.2.22 CRYSTAL OSCILLATORS AND TAPE SPEED SELECT LOGIC ⟨1⟩

The Crystal Oscillators provide stable and precise clock frequencies for 800, 556, and 200 bits-per-inch packing densities. The Tape Speed Select and Density Select logic divide the clock rates to the appropriate frequencies and select the Write Clock frequency which depends on tape speed and packing density. One set of crystals covers all standard tape speeds (from 12.5 to 112.5 ips) as well as most nonstandard tape speeds. The Speed Clock signal is used by the Delay Counter to provide all the precise time delays for the Formatter and is dependent only on tape speed.

4.2.23 DENSITY SELECT LOGIC ⟨2⟩

The Density Select logic provides control over selection of high- or low-density for 7-track Tape Units. Nine-track Tape Units are automatically operated only at 800 BPI. The Density Selection is normally controlled by the Computer program via the Hi Density Select signal but can be over-ridden by front panel switches. Different pairs of densities can be accommodated on multiple 7-track Tape Units; i.e., one unit can have densities of 800/556 BPI while a second unit can have densities of 556/200 BPI and a third unit can have densities of 800/200 BPI.

4.2.24 DATA TRANSFER CONTROL LOGIC ⟨10⟩

The Data Transfer Control logic operates in conjunction with the Read or Write Control logic, and depends on whether a Read or Write operation is active. The Read or Write Control logic generates the Set Data Flag pulse to signal that Read data is ready to input or to request a Write data character. For Write operations, the Controller returns the W/R ACK signal which clears the Data Flag and is used to strobe the Write data into the Write Storage Register. When the Controller desires to halt data transfer, it generates the HALT signal and the Data Flag signal is disabled.

4.2.25 DELAY COUNTER LOGIC (3)

The Delay Counter is a flip-flop divider chain that counts the Speed Clock pulses to provide precise time intervals for Predelays and Postdelays as well as Halt delays. The time interval is defined by the interval from the time the counter is allowed to start counting (from a reset condition) until the STOP signal is generated by a set of gates that decode various counts from the Delay Counter. The gate selected for a particular time interval is dependent on which State the Formatter is in as well as the configuration of the Formatter and the selected Tape Unit (provided by the STATUS signals to the Delay Counter).

4.2.26 INTER-RECORD GAP DETECT LOGIC (4)

The IRG Detector is used to trigger the Formatter from State 3 to the Post Delay State 4, or Halt Delay State 5 or 6, when completing any Read, Space, or Write operation with a dual-stack Read-After-Write Tape Unit. The IRG Detector resets the Delay Counter with each Read Strobe. When the Read Strobes are terminated, the Delay Counter is allowed to count for a prescribed interval until the STOP time is reached. When the STOP time is reached, State 3 is terminated.

4.3 COMMAND DESCRIPTIONS

The Formatter executes the following basic commands:

A. Read (one record)
B. Write (one record)
C. Space
D. Write File Mark
E. Erase 3-inch Gap
F. Rewind
G. Offline
H. Clear

4.3.1 COMMAND AND MODE COMBINATIONS

Table 4-3 lists the commands which it is possible for the Formatter to execute. Command execution depends on the mode lines.

TABLE 4-3. Command and Mode Combinations

FORMATTER OPERATION	COMMANDS													MODES				
OPERATION DESCRIPTION	REV*	WCC	WFM	GAP	FSR	RCC	CLR	REW	OFL	EDIT	TRD	STOP SPACE	CD	GEN ODD PAR	HI DENSITY	THR1	THR2
1. Test Read Forward						X					X		3				
2. Read Forward						X							3				
3. Read Reverse	X					X							3				
4. Write 1 Record (normal)		X															
5. Write 1 Record (Edit)		X								X							
6. Space Forward 1 record					X								3				
7. Space Forward n records					X							2	3				
8. Space Reverse 1 record	X												3	4	4	5	6
9. Space Reverse n records	X											2	3				
10. Space Reverse (edit mode)	X									X			3				
11. Write File Mark			X							1			3				
12. Erase 3-inch gap*				X													
13. Erase 3-inch gap then Write File Mark			X	X													
14. Erase 3-inch gap then Write 1 record		X		X													
15. Rewind								X									
16. Off-line									X								
17. Initiate Rewind then Offline								X	X								
18. Clear							X										

NOTES: * 7.62cm. Also applies to items 13 and 14.

1 The Edit mode can be used to rewrite a File Mark if the File Mark is first backspaced over in the Edit mode.

2 The STOP SPACE signal is used only for continuous spacing over multiple records. The RCAS signal can be used by the Controller to count records for determining when the required number of records has been traversed.

3 The Core Dump (CD) signal is ignored if 7-track, but can be used to Write and to check for 7-track-type File Marks on 9-track Tape Units; i.e, an octal 17 with even parity is written (and decoded as a File Mark when reading) instead of the normal octal 23 with odd parity. This provides compatibility with certain software of some existing computer manufacturers.

4 The GEN ODD PARITY and HI DENSITY mode lines are ignored when a 9-track Tape Unit is selected, or when the MODE switch on the OCP is in the MANUAL position regardless of whether a 7-track or 9-track Tape Unit is selected. If the MODE switch is in the REMOTE position and a 7-track Tape Unit is selected, the GEN ODD PARITY line controls whether odd or even parity is written or checked for; and the HI DENSITY line controls the written character packing density and the time period allowed between Read strobes in the RCAS circuits.

5 The THR1 mode affects only Tape Units having a single-stack Write/Read head. This mode line enables a marginal parity check to be performed on each record, immediately after it is written, by backspacing over the record and then spacing or reading forward in this mode while checking for parity error status.

6 The THR2 mode affects only Tape Units equipped with this option. It allows recovery of low-amplitude Read Data from tapes of low quality.

The Command signals are strobed into a Command storage register in the Formatter by the Command Clock (STROBEC); therefore, they can be changed immediately after the termination of the (STROBEC) pulse. The mode lines must be held static throughout each operation because no storage is provided in the Formatter.

4.3.2 READ AND SPACE COMMANDS

The Read and Space operations can be in the forward or reverse direction in any one of three possible modes:

A. Normal
B. Read Threshold High
C. Read Threshold Extra Low

In addition, a Read forward operation may be performed in a Test Read mode in which the CRC and LRC characters are not stripped from the data. The Read Threshold High mode is used with single-stack head (Read/Write) Tape Units to allow marginal checking of each record immediately after it is written by backspacing over the record and reading or spacing forward in the Read Threshold High mode, then checking for no parity errors. The Read Threshold Extra Low mode provides the ability to recover low-amplitude data from tapes of poor quality (if the Tape Unit is equipped with this option).

The Space operations can be for a single- or multiple-record under control of the STOP SPACE Controller signal. In addition, the backspace operation can be conducted in the Edit mode to correctly position the Write head in the IRG which precedes a record that is to be replaced with an equal length but updated record. BOT automatically halts backspacing.

4.3.3 WRITE, ERASE 3-INCH GAP, AND WRITE FILE MARK COMMANDS

The Erase 3-inch (7.62cm) Gap command can be performed alone or combined with the Write or Write File Mark command to cause a 3-inch (7.62cm) gap to be erased before the record or file mark is written. A Write command can be performed in the Edit mode (if the record to be replaced has first been backspaced over in the Edit mode to correctly position the head) to replace a record with an equal length record of updated information.

4.3.4 REWIND AND OFFLINE COMMANDS

The Rewind command causes the selected Tape Unit to rewind to Load Point (Beginning of Tape). The Formatter can optionally go Busy until the rewind is terminated (to provide a means of interrupting the Computer upon termination of the operation).

The Offline command never sets the Formatter to the Busy state and may be sent to a selected Tape Unit even if the Tape Unit is performing a Rewind operation and is Not Ready.

4.3.5 CLEAR COMMAND

The Clear command can be used to clear the Command and Status registers and set the Formatter to initial conditions even if the Formatter is Busy. After the Clear command is executed, the Formatter returns to the Not Busy status.

4.4 STATE FLOW

The State Counter controls the conditions through which the Formatter is sequenced; therefore, the State Counter achieves the proper timing relationships for various operations. The State Counter operational flow is described in the following paragraphs.

4.4.1 SIMPLIFIED STATE FLOW

Figure 4-3 illustrates, in simplified form, the State Counts that the Formatter sequences through while executing its various operations.

4.4.1.1 Initial Conditions. The Formatter is in Rest State 0 at initial conditions. The Strobec command clock is rejected if the command is not valid. If CBUSY is not set by a valid command, then one of the following commands must be entered:

A. Offline
B. Rewind (without interrupt)

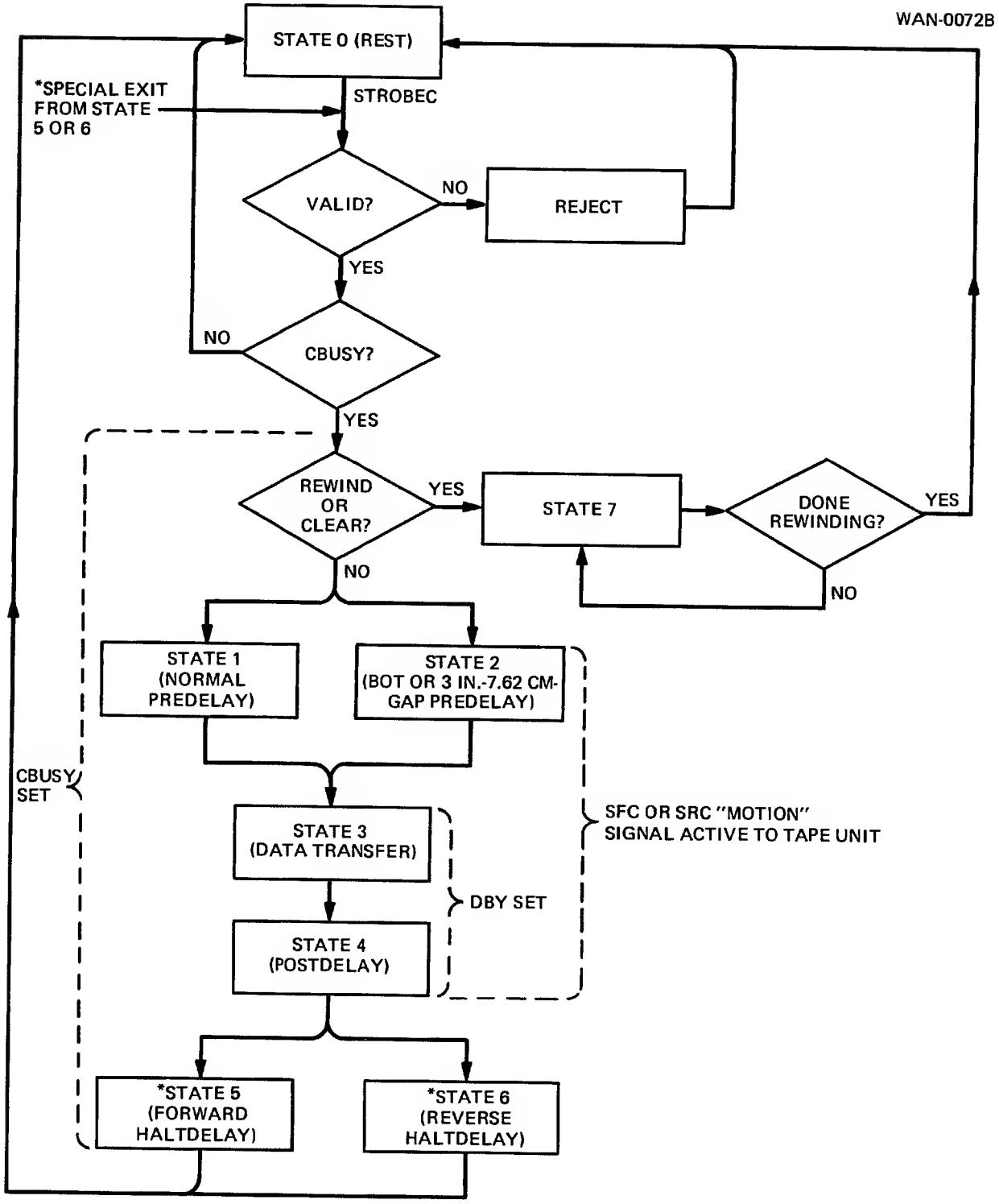


Figure 4-3. Simplified State Counter Flow Diagram

If either of these commands is entered, the command is executed but the Formatter remains in State 0. If CBUSY is set, then a Rewind or Clear command causes the Formatter to enter State 7 until the rewinding status signal is false. At this time, CBUSY is cleared and State 0 is reentered. For a Clear command (since the Rewind status bit is never true), CBUSY is cleared almost immediately. Any other command causes one of the two Predelay States to be entered. State 1 is normally used, but State 2 is used when the Formatter is at BOT or when a 3-inch (7.62cm) gap command is executed. The appropriate motion signal (SFC for forward motion, SRC for reverse motion) is activated at this time. The Predelay States are used to erase a 3-inch (7.62cm) gap or part of the IRG when writing, and to allow sufficant time for the Tape Unit to attain proper speed.

4.4.1.2 Data Transfer

The State 3 data transfer then takes place. For Write, the data is written until the HALT signal from the Controller terminates the record. For Erase, no data transfer is needed so State 3 is terminated immediately and State 4 is entered. For Write File Mark, no data transfer actually occurs, but the Formatter writes the File Mark and the LRC character and then enters State 4.

4.4.1.2.1 Delay. For dual-stack (Read-After-Write) Tape Units, the transition from State 3 to State 4 is delayed until the Read head detects the end of the record (the beginning of the IRG) to allow the full record to be checked for no parity errors. State 4 Postdelay (in conjunction with the 0.2-inch (5.08mm) distance the tape moves after the motion command terminates) is used to erase the first part of the IRG.

4.4.1.2.2 Reading or Spacing. For Reading or Spacing operation, State 3 is maintained until the end of the record and the IRG is reached. For reading, the Controller HALT signal terminates actual data exchange. For reading or spacing, the State 4 Postdelay (in conjunction with the fixed 0.2-inch (5.08mm) distance the tape moves when halting after the motion command terminates) is used to position the tape under the head in the correct position in the IRG to allow for a subsequent Write or Read operation.

NOTE

The Data Busy (DBY) signal is active only during States 3 and 4 while the motion signals to the Tape Unit are active from the beginning of the Predelay State through the Postdelay State.

4.4.1.2.3 HALT Delays. After the Postdelay occurs, one of the forward/reverse HALT delays (State 5 or 6) is entered to ensure that the tape is allowed sufficient time to come to a halt in the IRG. At the termination of the Halt Delay signal, CBUSY is cleared (to signal the Computer that the next command can be executed) and Rest State 0 is entered.

4.4.1.2.4 Special Exit. The Special Exit from State 5 or 6 allows continuous writing or reading without stopping in the IRG. Therefore, the Special Exit optimizes the efficiency of data transfer. Since the Start/Stop characteristics of the Tape Units are ramp-like, the gap-traverse time is twice as long if the next command is delayed until the tape has completely halted (compared to On-the-Fly operation). With CBUSY active in any other State, any command except Clear is rejected.

4.4.1.2.5 Restrictions. The Computer can accomplish On-the-Fly Write or Read operations by initiating the next command when DBY terminates at the end of State 4, rather than waiting until CBUSY terminates; however, there are certain restrictions on this type of operation. It is the responsibility of the Computer program to ensure compliance with the following restrictions:

A. The next command must not switch from a Write or Write File Mark to a Space or Read, or vice versa.
B. The next command must not change direction of motion.
C. The next command must not be a Rewind or Offline command if the previous command was a Write or Write File Mark command.

NOTE

The Delay Counter is used in States 1, 2, 4, 5, and 6 to generate the prescribed delay times.

4.4.2 DETAILED STATE FLOW

Figure 4-4 shows the control over signals DBY and CBUSY, and motion commands SFC, SRC as well as the use of the Delay Counter. In addition, the IRG detection exit from State 3 is detailed, as is the detour around State 4 Postdelay (to achieve minimum Postdelay) in certain cases.

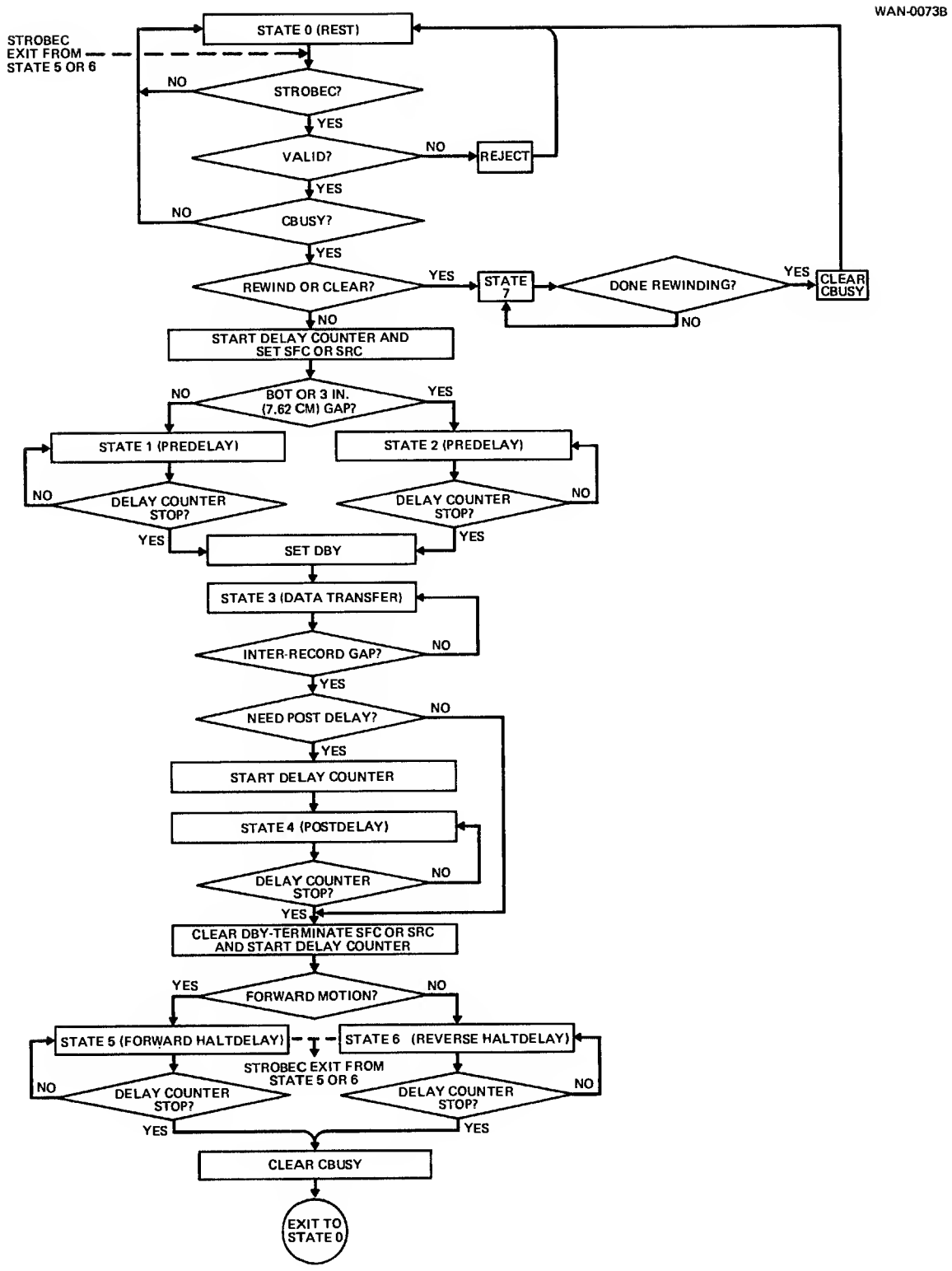


Figure 4-4. Detailed State Counter Flow Diagram

4.5 COMMAND EXECUTION AND TIMING

The following main commands and their associated timing diagrams are discussed step-by-step in the succeeding paragraphs:

A. Clear
B. Rewind (with interrupt)
C. Write file mark (7-track)
D. Write file mark (9-track)
E. Forward space 1 record
F. Backspace 1 record
G. Write 1 record (7-track)
H. Write 1 record (9-track)
I. Read 1 record (7-track)
J. Read 1 record (9-track)
K. Erase 3-inch (7.62cm) gap.

4.5.1 CLEAR COMMAND FUNCTION

The Clear command terminates any motion command and resets the Formatter to initial conditions. CBUSY sets and then resets after the Clear command is complete. This signifies the Formatter is ready for the next command. The timing diagram for the Clear command is shown in Figure 4-5.

The Clear command is included mainly to allow diagnostic programs control over a faulty Formatter that does not halt the Tape Unit. This command must not be used to halt any Write or Read operation, because it does not halt the head at the correct point in the IRG and the CRC/LRC characters cannot then be written or read. The System Reset (SRS) pulse resets the Status register upon acceptance of a valid command.

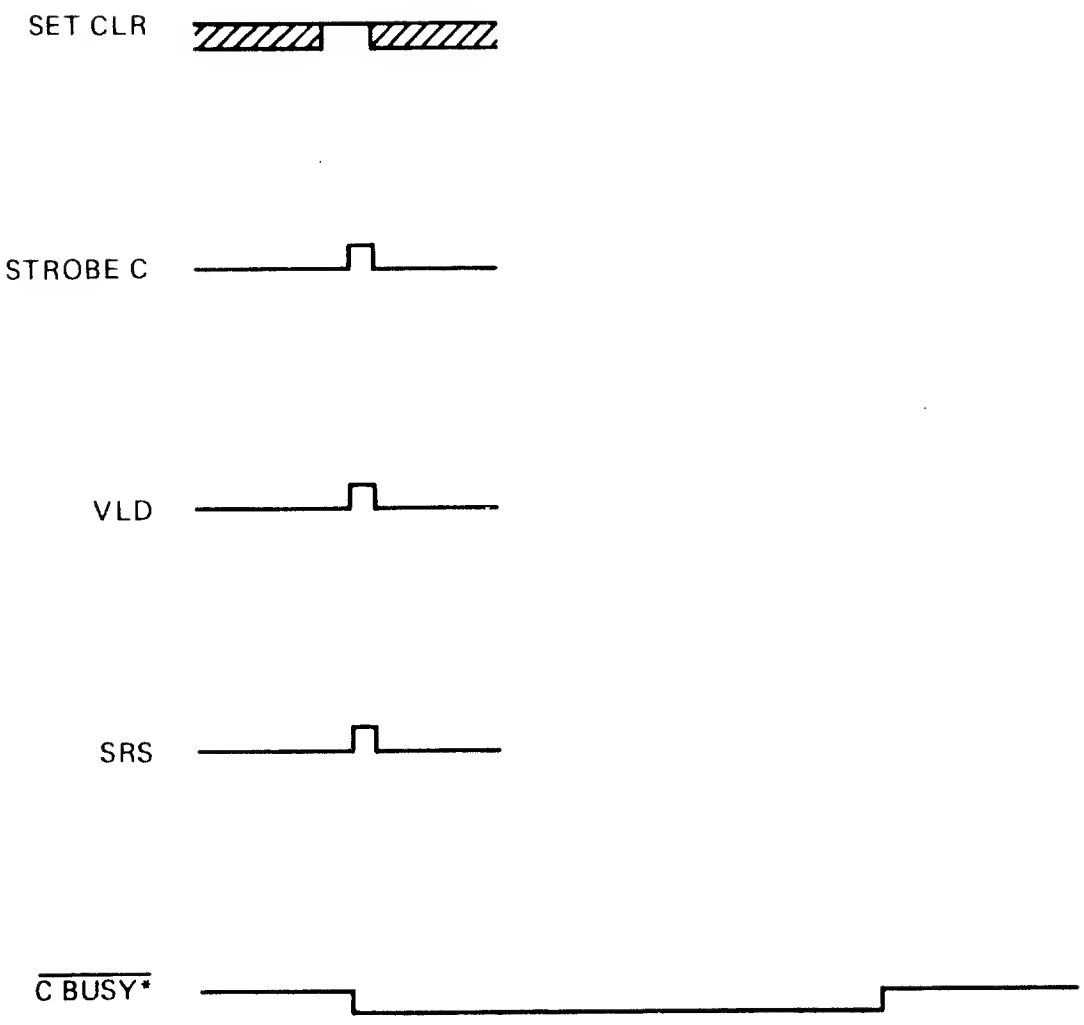


Figure 4-5. Clear Command Timing Diagram

4.5.2 REWIND COMMAND (WITH INTERRUPT)

Neither the Offline or Rewind command can set CBUSY if the Rewind Interrupt is jumpered out. In this event, the commands are passed on to the selected Tape Unit as a pulse. If jumper E1 to E2 is missing on the NRZI Control board (Assy. 201659), then CBUSY is set for a Rewind command and resets when the Rewind command is completed. This signals the Computer that the next command can be accepted by the Tape Unit.

Figure 4-6 illustrates the timing of the Rewind command with Interrupt. When the Controller generates the STROBEC pulse while SETREW is high and the Formatter is not busy, the command is accepted and the VLD pulse is generated.

The REW F-F is set to store the Rewind command. When the STROBEC clock pulse terminates, the Rewind command is generated to the selected Tape Unit (signal $\overline{\text{RWC}}$). When the Tape Unit responds that it is rewinding (signal REWINDING) the REW F-F is reset and the Formatter $\overline{\text{RWDG}}$ status bit is set. The Tape Unit goes not ready ($\overline{\text{RDY}}$) during a rewind. Since the Tape Unit rewind terminates before the Tape Unit returns to load point and becomes Ready again, the $\overline{\text{RWDG}}$ status bit is interlocked to wait until the Tape Unit goes Ready (RDY). The SRS pulse resets (clears) the Status register upon acceptance of a valid command. $\overline{\text{CBUSY}}$* is reset to signal that the operation is complete.

4.5.3 WRITE FILE MARK COMMAND (7-TRACK)

When signal SET WFM is high during the STROBED clock pulse, the WFM command register F-F is set to initiate a Write File Mark command. The SRS pulse is also generated to reset the Formatter to initial conditions. The CBUSY F-F is set by the VLD clock, and the $\overline{\text{SFC}}$ command is activated to start the tape moving in the forward direction. The Write amplifiers in the selected Tape Unit are enabled and the $\overline{\text{WARS}}$ signal is high. Command register F-F WFM also sets the selected Tape Unit to the Write mode via the $\overline{\text{SWS}}$ signal. The Predelay signal delays writing of the file mark character until the Tape Unit is up to speed and has generated a portion of the required IRG. If the Tape Unit is at BOT when the Write File Mark command is generated, the Predelay period is longer to cause a 3-inch (7.62cm) gap to be erased before the file mark is written. The Enable Write Data Request (EWDR) F-F is set upon the termination of the Predelay signal. The Write Data Clock (WDCL) F-F is set one write-clock period later, and is gated to set the Enable Blank Character Counter (EBCC) F-F. The EWDR F-F is immediately reset. This causes F-F

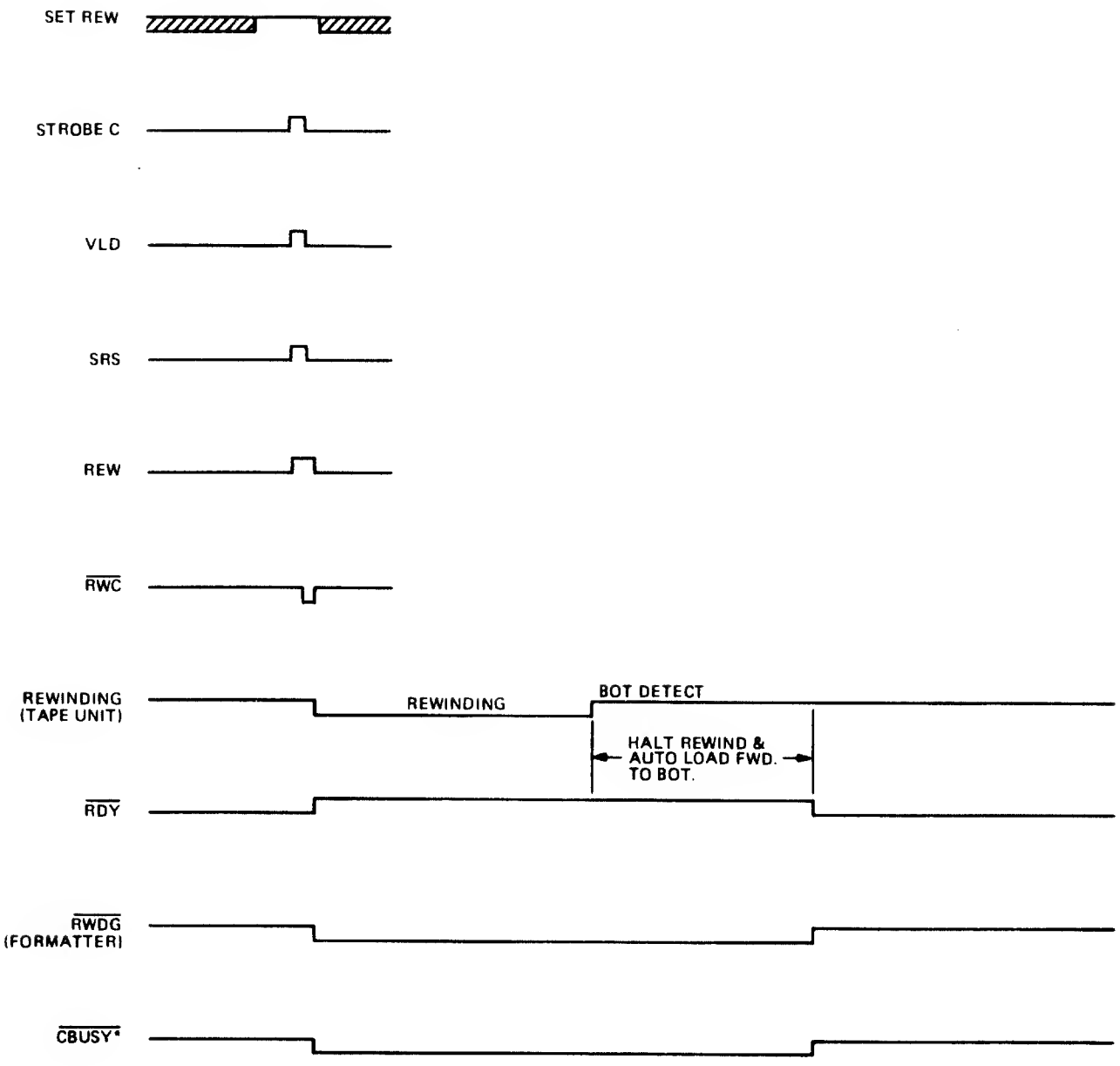


Figure 4-6. Rewind Command Timing Diagram

WDCL to be reset one write-clock period later; thus, only one Write Data Strobe (WDS) pulse is generated to the selected Tape Unit. The Command register F-F WFM gates the file-mark code onto the data bus. The timing diagram for the Write File Mark command is shown in Figure 4-7.

4.5.3.1 Blank Character Count. The blank character counter (comprised of F-F's CC1, CC2 and CC4) begin counting from the occurrence of the Write File Mark clock to cause the WARS F-F's to be set which resets the Tape Unit Write Amplifier F-F's to cause the LRC character to be written. The Tape Unit continues running in the forward direction until the File Mark passes under the Read head so that the file mark and LRC character can be checked for vertical parity and longitudinal parity. The time interval (in milliseconds) between writing the File Mark and reading back the File-Mark character, is equal to 150 divided by the tape speed in inches-per-second (ips) or 2.54 centimeters per second. As the timing diagram illustrates, the read data strobe ($\overline{RDS}$) occurs, and 8 character times later (for 9-track Tape Units), the LRC character Read Strobe occurs. The LRC character occurs 4 character times later for 7-track Tape Units. The RCAS is set upon detection of the first $\overline{RDS}$ pulse and times out 2- or 3-clock periods later. While the RCAS circuit is active, the character parity is checked.

4.5.3.2 Delay Counter. The Delay Counter is reset by each Read Strobe and then times out a delay interval after the last Read Strobe; therefore, the Delay Counter performs the task of IRG detection. Upon termination of the Delay Counter time out, the STOP pulse is generated and used to check for an LRCC error in the previous record. The STOP pulse is also used to trigger the State 4 Postdelay circuits (S4). When the Postdelay terminates, the $\overline{SFC}$ signal is terminated and the State 5 Halt Delay is entered. The Halt Delay ensures that the Tape Unit is guaranteed to have ceased all motion in the IRG. If the next command is to be a Write-type command, then the IRG can be erased On-the-Fly at full tape speed without stopping in the IRG by issuing the command after $\overline{DBY}$ terminates rather than waiting until $\overline{CBUSY}$ terminates. Status is valid after DBY terminates; therefore, the status can be checked before the next command is issued.

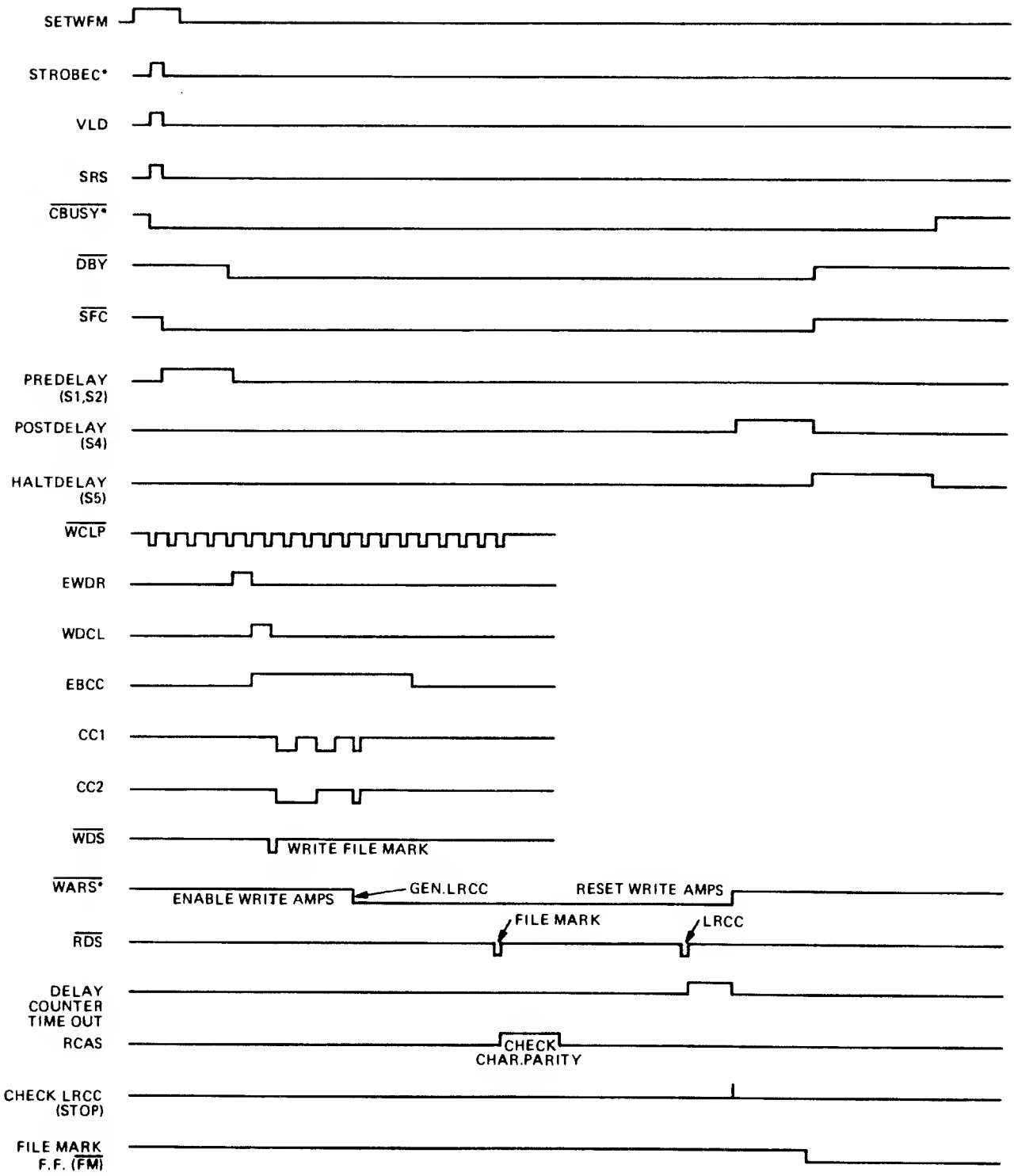


Figure 4-7. Write File Mark Command Timing Diagram (7-Track)

4.5.4 WRITE FILE MARK COMMAND (9-TRACK)

Writing a File Mark in 9-track mode is similar to the 7-track mode, except 8 character times separate the File Mark and the LRC character.

NOTE

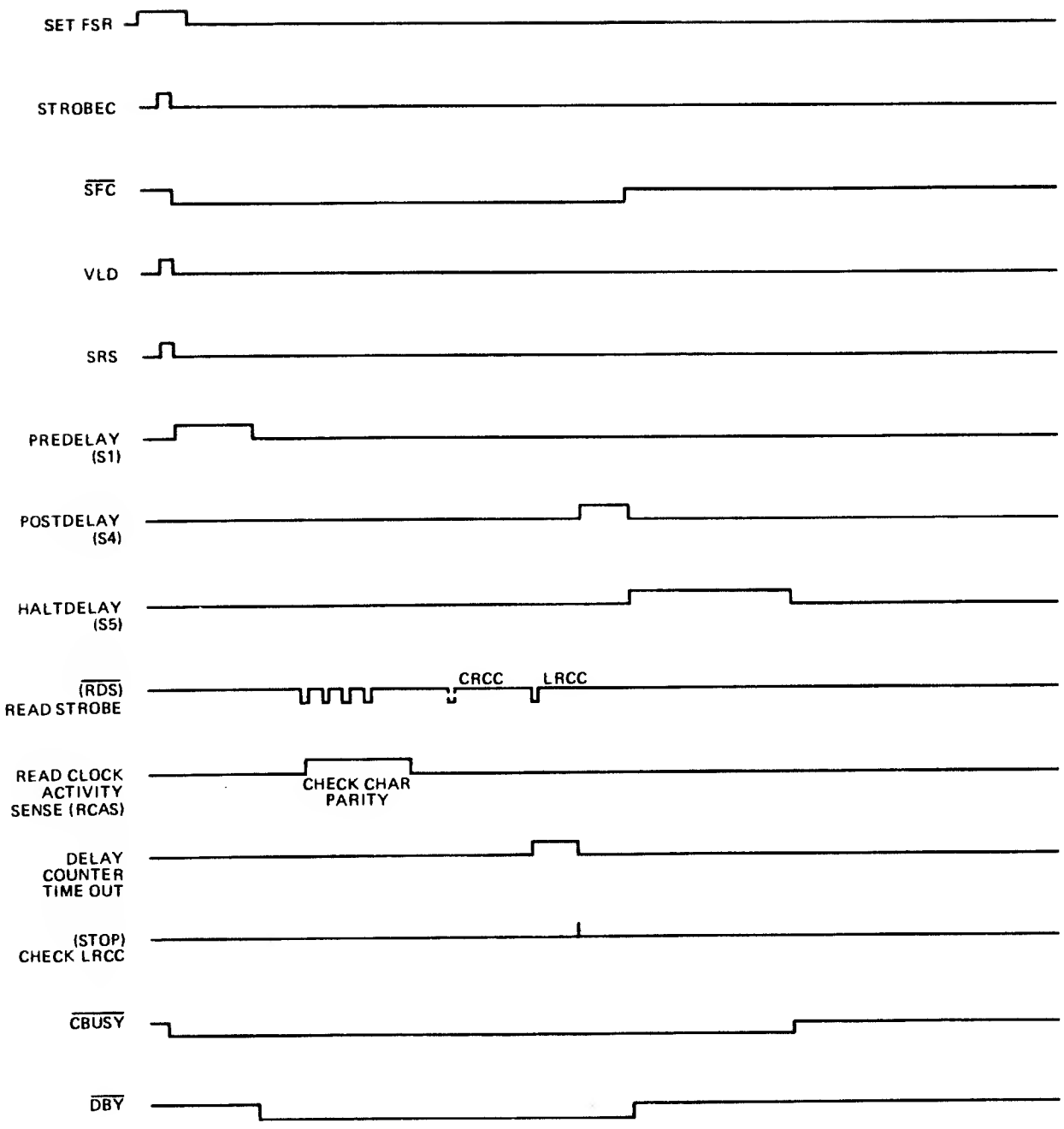
Effectively, there is an all-zeros CRC character because in data records the CRCC occurs at the fourth character time; then four character times later the LRCC is written.

4.5.5 FORWARD SPACE/RECORD COMMAND

When the term SET FSR and the STROBEC pulse are simultaneously high, the $\overline{\text{SFC}}$ signal is activated to move tape forward as shown in Figure 4-8. The VLD and SRS pulses are generated to reset the Formatter and initiate the Space Forward operation.

NOTE

The Space Forward Command results in spacing over ONE record if signal STOP SPACE is open-circuited or at the high level. If multiple records are to be spaced over, STOP SPACE must be held low until the leading edge of the $\overline{\text{RCAS}}$ signal occurs for the last record. The $\overline{\text{RCAS}}$ signal may be used to count records to determine when the last record to be spaced over is reached, but the leading edge of the RCAS signal should be used to provide control over signal STOP SPACE as indicated. The $\overline{\text{FM}}$ status signal and $\overline{\text{EOTS}}$ status signal may also be used to switch STOP SPACE high so that a File Mark or the End-of-Tape can halt the multiple record spacing operation. For multiple spacing operations, $\overline{\text{CBUSY}}$ remains low until the final record has been passed.



1. CRCC MAY BE MISSING FOR 9-TRACK TAPE UNITS AND IS ABSENT ON 7-TRACK TAPE UNITS.

Figure 4-8. Forward Space One Record Timing Diagram

The Predelay allows the Tape Unit to attain proper speed before allowing Read Strobe pulses to be accepted. The Read Strobe pulses activate RCAS to enable parity checks to be made while spacing. When the record is past, the Delay Counter times out to detect the IRG; then the LRCC check is made. After the $\overline{\text{DBY}}$ signal terminates, status can be checked and the next command can be issued (if a Read or Space Forward) to accomplish On-the-Fly operation. If no new command is issued at this time, the normal Halt Delay sequence is entered.

4.5.6 BACKSPACE/RECORD COMMAND

The Backspace command is similar to the Forward Space command, except the LRC/CRC characters occur first (ref. figure 4-8).

4.5.7 WRITE ONE RECORD COMMAND (7-TRACK)

The Write One Record command causes the Tape Unit to turn on the Write current, enable the Write amplifiers, attain proper speed, generate a portion of the IRG, then request output data transfers from the Controller as shown in Figure 4-9. The requested data characters are written on tape until a HALT signal is generated by Controller logic. The HALT signal terminates the record by writing the CRC character (9-track Tape Units only) followed by the LRC character. The Tape Unit Read-After-Write head enables parity checks to be performed upon the record that has just been written. After the parity checks are completed, the Tape Unit erases a portion of the next IRG and is then commanded to halt. After sufficient time has elapsed to ensure that tape motion has completely stopped, the completion of the Write One Record command is signaled when $\overline{\text{CBUSY}}$ terminates. On-the-Fly generation of the IRG without stopping may be accomplished by checking status at the termination of signal $\overline{\text{DBY}}$ and immediately issuing the next Write, Erase or Write File Mark command. The Write mode is set by the command clock (VLD) to initiate the Write One Record command. The System Reset (SRS) pulse is also generated by VLD to reset the Controller to initial conditions. The $\overline{\text{CBUSY}}$ F-F is set by VLD to initiate the Write One Record command. The Synchronous Forward $\overline{\text{SFC}}$ signal is then sent to the Tape Unit to initiate forward motion.

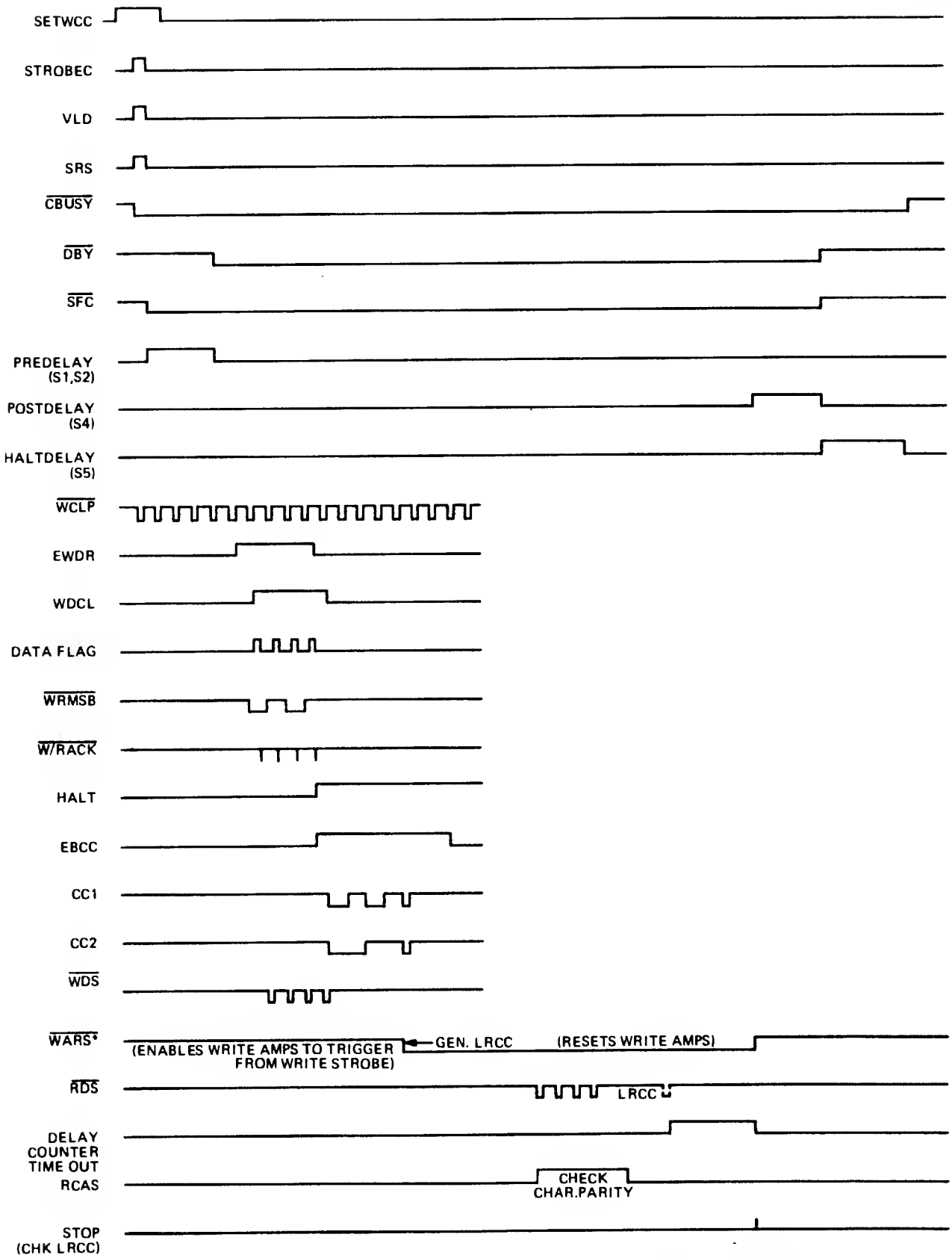


Figure 4-9. Write One Record Command Timing Diagram (7-Track)

4.5.7.1 Predelay Time Out. After the Predelay (S1, S2) times out, the EWDR F-F is clocked set to begin writing the record. Predelay erases the last portion of the IRG as the Write current is on for this period. The WDCL F-F is clocked set one clock time after the EWDR F-F. This enables Write Data Strobe (WDS) pulses to be generated to the Tape Unit.

4.5.7.2 Data Flag. The first Data Flag signal is sent to the Controller. When the Controller has the first character ready to transfer, it generates the $\overline{\text{W/R ACK}}$ pulse which stores the first output character in the Formatter Write Data Register and clears the Data Flag. The first $\overline{\text{WDS}}$ is then generated by the next $\overline{\text{WCLP}}$ signal to clock the character stored in the Write Data Storage Register onto the magnetic tape. At the trailing edge of the $\overline{\text{WDS}}$ pulse, the Data Flag is set to request the next character from the Controller.

4.5.7.3 CRC Generator Register. The $\overline{\text{WDS}}$ pulse is OR gated with an extra CRC clock-generation signal to clock the CRC Generator Register (ref. logic diagram ⟨16⟩) to begin calculation of the CRC character. The CRC Generator Register is initially reset. The CRC Generator Register then monitors the Write Data output bus to generate a check character that is unique for the data characters written on tape. If the output data character is not transferred to the Controller before the next $\overline{\text{WDS}}$ pulse occurs, a timing error status bit is set. The sequence of Data Flag—W/R ACK—$\overline{\text{WDS}}$ continues until the HALT signal is generated by the Controller to terminate the writing. The HALT signal sets the enable-blank-character-counter (EBCC) F-F. The EBCC F-F enables the Blank Character Counters CC1, CC2, and CC4, disables the Write control F-F's, and resets the Write Most Significant Byte (WRMSB) F-F.

4.5.7.4 Blank Character Counters. The Blank Character Counters control the generation of the CRC and LRC characters to generate the end of the record. These counters are decoded in the 9-track mode to create an extra CRC clock and to gate the contents of the CRC generator onto the Write Data output bus. The contents of these Blank Character Counters are also decoded to set the WARS F-F which in turn resets the Write Amplifiers via the $\overline{\text{WARS}}$ signal. This generates the LRC character.

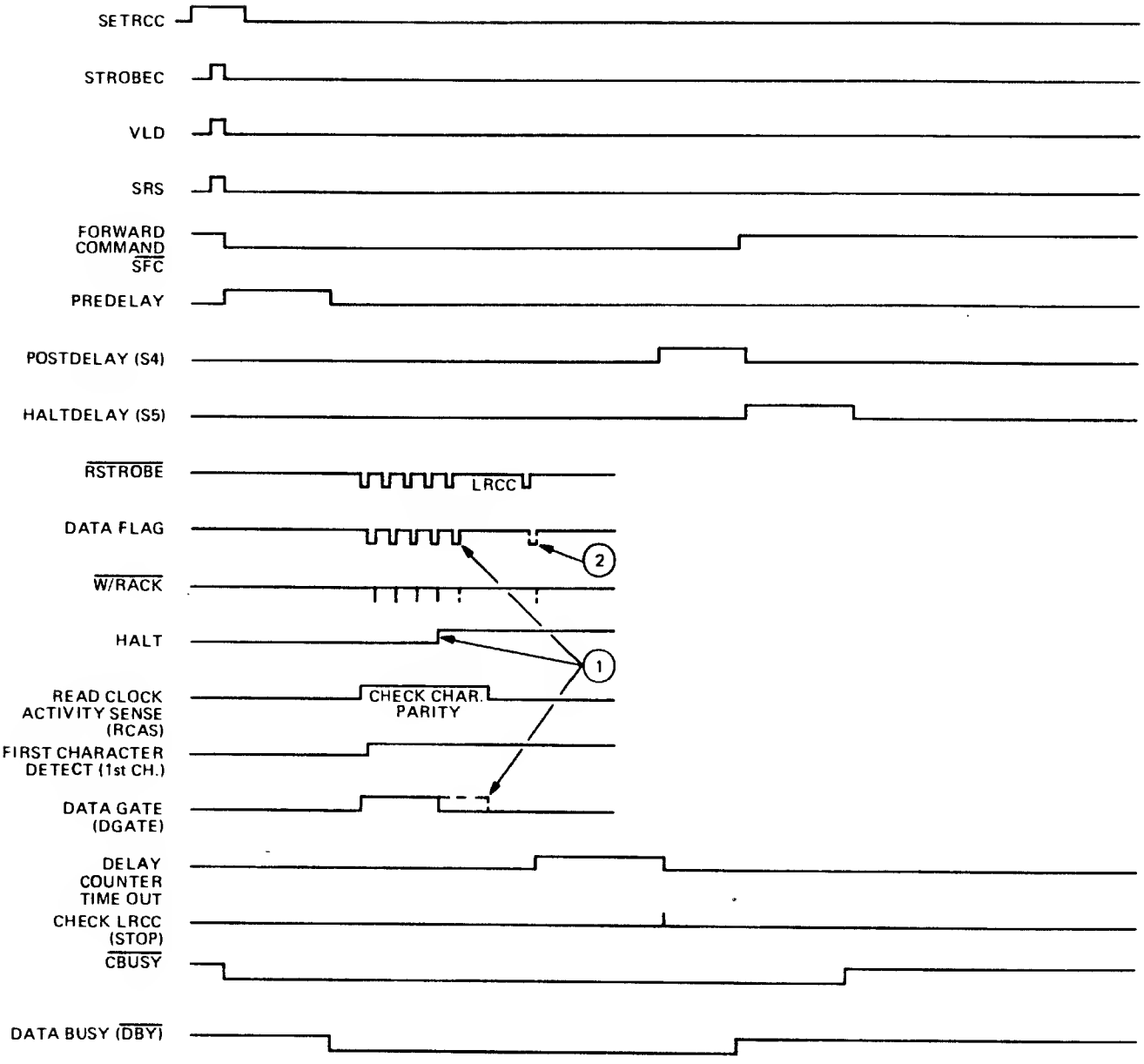
4.5.7.5 Parity Check. The Tape Unit continues motion in the forward direction so that the Read-After-Write head can check parity of the entire record. The Read Data Strobe ($\overline{RDS}$) pulses trigger the Read Clock Activity Sensor circuit (1-RCAS) which defines the characters that are to be checked for vertical parity. Two or three clock periods after the last character in the record is read, the RCAS signal terminates and vertical parity checking is disabled. The Delay Counter times out after the LRC character is detected at the end of the record to provide detection of the IRG. The STOP pulse is then used to check for an LRC error. The Postdelay time out interval ensures that a sufficient portion of IRG is erased in the forward direction after a record is written. This enables the Tape Unit to start in the reverse direction and attain proper speed for a backspace Read operation. At the end of the Postdelay, the $\overline{SFC}$ command terminates and the Halt Delay begins timing out to ensure the tape has come to a complete halt before $\overline{CBUSY}$ terminates. For continuous On-the-Fly writing (no stopping in the IRG), the status can be inspected after $\overline{DBY}$ terminates; then a Write, Erase, or Write File Mark command can be immediately issued.

4.5.8 WRITE/RECORD COMMAND (9-TRACK)

Writing in the 9-track mode is similar to that of the 7-track mode (ref. figure 4-9), except there is a Cyclic Redundancy Check Character (CRCC) written four character times after the end of the record; the CRCC is then followed by the Longitudinal Redundancy Check Character (LRCC) four character times later.

4.5.9 READ ONE RECORD COMMAND (7-TRACK)

The Read One Record command is initiated when the SET RCC and the STROBEC pulse are simultaneously high as shown in Figure 4-10. VLD sets the RCC F-F in the Command register. SRS is generated by the VLD clock to reset the Formatter to initial conditions. The $\overline{SFC}$ command and the $\overline{CBUSY}$ signal are activated at the same time. After a Predelay interval to allow the tape to attain proper speed, Read Data Strobe pulses to the Read logic are enabled. The first Read Data Strobe pulse that occurs sets the data gate (DGATE) F-F and triggers RCAS. The trailing edge of the first Read Data Strobe pulse sets the First Character Detect (1st CH) F-F which, in turn, disables any further Read Data Strobe pulses from setting the DGATE F-F. When the end of the record is reached, the RCAS circuit times out two or three character times later. This resets the DGATE F-F if the Computer has not already terminated data transfer (via the HALT signal).



NOTES

2. IF "TEST READ MODE", THE DATA FLAG ALSO OPERATES FOR THE LRC CHARACTER TO INPUT IT TO THE COMPUTER.
1. IF "HALT" DOESN'T OCCUR BEFORE END OF RECORD, THE DATA GATE WILL REMAIN SET AND THE DATA FLAG WILL CONTINUE OPERATION.

Figure 4-10. Read One Record Command Timing Diagram (7-Track)

4.5.9.1 Read Data Transfer. During the interval when the DGATE F-F is set, data transfer takes place. During the time that RCAS is set, the characters are checked for parity. The CRC/LRC characters are not checked for parity. If the HALT signal occurs before the end of the record, the DGATE F-F is reset to terminate Data Flag requests.

NOTE

The dashed line signals of figure 4-10 annotated by Note 1 illustrate that if the HALT signal is missing, the fifth tape character shown on the timing diagram is input to the Computer and the DGATE F-F does not reset until the RCAS circuit times out at the end of the record. The dashed waveforms annotated by Note 2 indicate that the Data Flag operates for the CRC and LRC characters when the record is read in the Test Read mode.

4.5.9.2 Timing Out. The Test Read mode is provided so that the CRC/LRC characters can be read into the Computer for diagnostic purposes. Regardless of whether the Read One Record command is or is not terminated by a HALT, tape motion continues until the IRG is reached, at which time the Delay Counter begins timing out. When the IRG is indicated by the Delay Counter time out, the LRC check logic is strobed by the STOP pulse and causes the parity error status F-F to set if an LRCC error exists. The Postdelay interval is then entered (S4) at the end of which the $\overline{\text{SFC}}$ command to the Tape Unit is terminated. The Halt Delay (S5) then begins timing out to delay reset of the $\overline{\text{CBUSY}}$ signal until the Tape Unit has completely halted all tape motion. If continuous read (no stopping in the IRG) is desired, then termination of $\overline{\text{DBY}}$ can be used to signal that status is ready to be checked so that if the next command is for a Read or Space operation in the same direction it can be immediately issued.

4.5.9.3 Read Data Transfer Sequence. The signals for Read Data transfer are processed in the following sequence:

A. Pulse $\overline{\text{RSTROBE}}$ indicates Read data are being stored in the Formatter Read Data Register. The Read data are settled by the end of the pulse. At the trailing edge of the pulse, $\overline{\text{DATA FLAG}}$ is set.

B. When $\overline{\text{DATA FLAG}}$ goes low, a Read data transfer is requested.

C. After the Computer has accepted the data, pulse $\overline{\text{W/R ACK}}$ must be issued to clear the Data Flag.

D. The HALT signal (or the detection of the IRG) resets DATA GATE to terminate Read data transfer requests. HALT should be presented with the last $\overline{\text{W/R ACK}}$ pulse (or shortly thereafter).

The $\overline{\text{DATA FLAG}}$ signal reset has a built-in delay from the $\overline{\text{W/R ACK}}$ pulse such that the $\overline{\text{DATA FLAG}}$ signal can be gated to form the $\overline{\text{W/R ACK}}$ pulse when designing a Controller that packs two tape characters into one Computer word. Normally, a pulse from the Computer is used to generate the $\overline{\text{W/R ACK}}$ signal.

4.5.9.4 Toggle F-F. The leading edge of the $\overline{\text{RSTROBE}}$ pulse may be used to toggle a binary F-F on the Controller to determine whether the tape character is odd or even for Packing purposes. By using the leading edge, the toggle F-F can be gated with $\overline{\text{DATA FLAG}}$ to form the W/R ACK pulse on the odd characters while storing the odd characters in a Controller register. The toggle F-F can then be checked at the $\overline{\text{CKWDCNT}}$ pulse time to detect an odd number of characters in the record; i.e., to force a data transfer to the Computer for the extra odd character because Packing logic normally expects an even number of characters. In this way, a data transfer to the Computer normally occurs after every even character.

4.5.10 READ ONE RECORD COMMAND (9-TRACK)

The Read One Record (9-track) command is similar to the Read One Record (7-track) command, except that there can be a CRC character as well as a LRC character. The CRC character can be all zeros but there is always an LRC character (ref. figure 4-10).

4.5.11 ERASE 3-INCH GAP COMMAND

Timing for the Erase 3-Inch (7.62cm) Gap command is similar to the Write File Mark timing, except S2 operates the Predelay and no writing occurs (ref. figure 4-7).

4.6 CONTINUOUS (ON-THE-FLY) WRITE OR READ

Continuous Write allows the IRG to be generated at fully rated tape speed. If successive Write commands are based upon the termination of the CBUSY command (as is normal) then the tape comes to a full stop in the IRG. Similarly, continuous Read or Space allows the IRG to be traversed at fully rated tape speed. Data transfer cannot take place in the IRG, because this mode of operation optimizes the usage of the Tape Units by minimizing the amount of dead time. To obtain continuous On-the-Fly operation, the DBY signal may be used instead of the CBUSY signal as long as the following conditions are met:

A. The next command may not switch from a Read mode to a Write mode or vice versa.
B. The next command may not switch tape direction.
C. A Rewind or Offline command may not follow a Write or Write File Mark command.

A Write or Write File Mark command can follow a Write or Write File Mark command as soon as DBY terminates rather than waiting until signal CBUSY terminates. Similarly, a Read or Space Forward command can follow the same type command upon termination of DBY. A Read or Space Reverse command can follow the same type command upon termination of DBY.

4.7 OPTIONS

The following field-changeable options are provided in the Formatter:

A. Tape Speed Selection
B. 7-Track Density Pairing (800/556; 556/200; 800/200 Selection)
C. Single/Dual Head Stack Selection
D. BCD 10 to Zero Conversion (for Reading 7-track, Even Parity Tapes)
E. Zero to BCD 10 Conversion (for Writing 7-track, Even Parity Tapes)
F. Write and Read 7-track File Mark Code on 9-Track Tapes
G. No Parity Error for File Mark
H. No Interrupt for Rewind Command
I. Formatter Address Selection
J. Disable Manual Control
K. Manual Control of Density while MODE Switch Defines How Parity is Controlled
L. Automatic Selection of ODD Parity when a 9-Track Unit is Selected

4.7.1 TAPE SPEED SELECTION

The Tape Speed Selection option allows selection of any two tape speeds, by providing control over the Tape Speed Clock and Write Clock Generators (F-F divider chains). The selection is accomplished by controlling the division modulo of the F-F divider chain by loading the negative 2's complement of the divisor (divisor -1), whereupon the counter counts up to zero recycle. Chip position F5 on the Clock Generator card assembly is provided as a plug-in wire-wrap socket for this purpose. Input Pins 1, 2, 3, and 4 represent the four Tape Units A, B, C, and D, respectively. All Tape Units at speed 1 must have their input pins bussed together (call this bus 1) and all Tape Units at speed 2 must have their input pins bussed together (call this bus 2). To obtain the desired division ratio, Bus 1 must then be jumpered to Field 1 pins 5, 6, 7, 8, and 9 as indicated in Table 4-4. To obtain the second desired division ratio, Bus 2 must be jumpered to Field 2 pins 11, 12, 13, 14, and 15 as indicated in the table. These connections are shown in Figure 4-11. All remaining pins in Fields 1 and 2 must be jumpered to pin 16.

NOTE

Column 5 in table 4-4 gives the frequency of the Speed Clock used by the Delay Counter for time interval calculations. Columns 6, 7, and 8 give the Write Clock frequency for the tape speed. The Write Clock frequency depends on the bit packing density of the selected Tape Unit.

4.7.2 7-TRACK DENSITY PAIRING

The Formatter is configured to operate at 800 BPI with no jumpers in the Density Field on the Clock Generator card assembly or when a 9-track Tape Unit is selected. Different pairs of densities can be selected for different 7-track Tape Units; i.e., Tape Unit A could be 800/556 BPI; Tape Unit B could be 556/200 BPI; Tape Unit C could be 800/200 BPI; and Tape Unit D could be 800/556 BPI. The H pin for each 7-track Tape Unit must be jumpered to the 556 bus if the higher density of the pair is 556 BPI. The H pin can be ignored if the higher density is 800 BPI. The L pin for each 7-track Tape Unit must be jumpered to the 556 BPI or to bus the 200 BPI bus. This depends on the lower density of the pair. Figure 4-12 shows an example of density selection wiring.

TABLE 4-4. Tape Speed Selection (Continued)

Column 1		Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8
Tape Speed		Division Ratio	NEG.2's Complement	BINARY BIT WEIGHT 16 8 4 2 1 FIELD 1 PINS (F5) 9 8 7 6 5 FIELD 2 PINS (F5) 15 14 13 12 11	SPDCLK FREQ KHz (PIN D5-11)	WRITE CLOCK FREQ, KHz (PIN D5-5)		
(IPS)	(CMPS)					800 BPI	556 BPI	200 BPI
112.5	285.75	2	–1	0 1 1 1 1	22.5	90	62.55	22.5
75	190.5	3	–2	0 1 1 1 0	15	60	41.7	15
56.25	142.875	4	–3	0 1 1 0 1				
45	114.3	5	–4	0 1 1 0 0	9	36	25.02	9
37.5	95.25	6	–5	0 1 0 1 1	7.5	30	20.85	7.5
32.14	81.6356	7	–6	0 1 0 1 0				
28.125	71.4375	8	–7	0 1 0 0 1				
25	63.5	9	–8	0 1 0 0 0	5	20	13.9	5
22.5	57.15	10	–9	0 0 1 1 1				
20.45	51.943	11	–10	0 0 1 1 0				
18.75	47.625	12	–11	0 0 1 0 1				
17.3	43.942	13	–12	0 0 1 0 0				
16.07	40.8178	14	–13	0 0 0 1 1				
15.0	38.1	15	–14	0 0 0 1 0				
14.06	35.7124	16	–15	0 0 0 0 1				
13.23	33.6042	17	–16	0 0 0 0 0				
12.5	31.75	18	–17	1 1 1 1 1	2.5	10	6.95	2.5

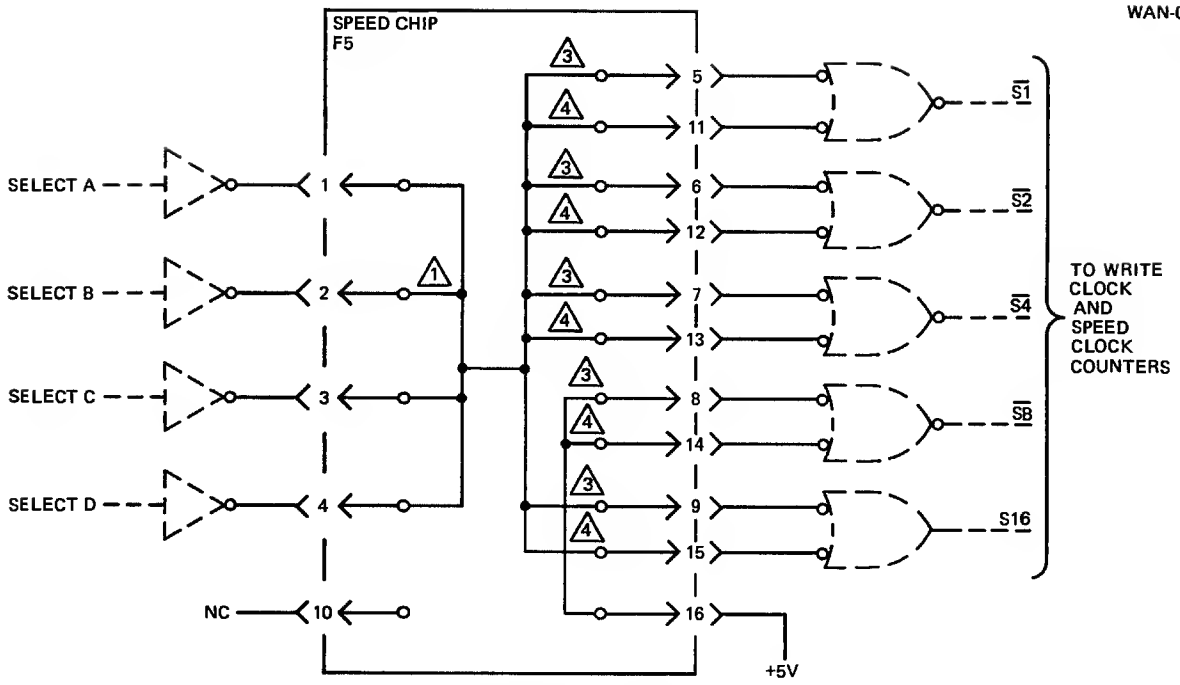
TABLE 4-4. Tape Speed Selection (Concluded)

Column 1		Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8
Tape Speed		Division Ratio	NEG.2's Complement	BINARY BIT WEIGHT 16 8 4 2 1 FIELD 1 PINS (F5) 9 8 7 6 5 FIELD 2 PINS (F5) 15 14 13 12 11	SPDCLK FREQ KHz PIN D5-11)	WRITE CLOCK FREQ, KHz		
(IPS)	(CMPS)					800 BPI	556 BPI	200 BPI
11.84	30.0736	19	–18	1 1 1 1 0				
11.25	28.575	20	–19	1 1 1 0 1				
10.7	27.178	21	–20	1 1 1 0 0				
10.22	25.9588	22	–21	1 1 0 1 1				
9.7	24.638	23	–22	1 1 0 1 0				
9.38	23.8252	24	–23	1 1 0 0 1				
9.0	22.86	25	–24	1 1 0 0 0				
8.6	21.844	26	–25	1 0 1 1 1				
8.3	21.082	27	–26	1 0 1 1 0				
8.03	20.3962	28	–27	1 0 1 0 1				
7.77	19.7358	29	–28	1 0 1 0 0				
7.5	19.05	30	–29	1 0 0 1 1				
7.2	18.288	31	–30	1 0 0 1 0				
7.03	17.8562	32	–31	1 0 0 0 1				

NOTES:

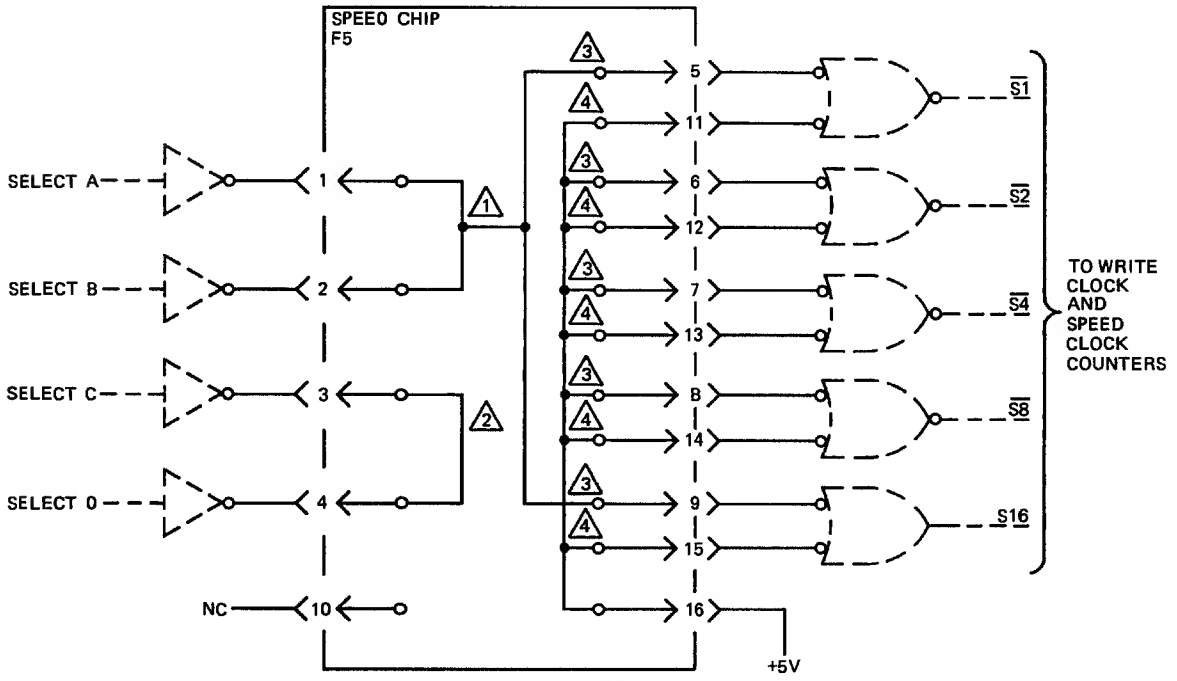
1. In Col 4, pins marked "0" must be jumpered to Bus 1 or 2, pins marked "1" must be jumpered to Pin F5-16 to enable.

2. Standard tape speeds are underlined.



All Tape Units at 25 ips (63.5 cm/sec)

EXAMPLE A



Tape Units A and B are 75 ips (190.5 cm/sec)

Tape Units C and 0 are 12.5 ips (31.75 cm/sec)

EXAMPLE B

NOTES (1) = Bus 1 ; (2) = Bus 2 ; (3) = Field 1 ; (4) = Field 2

Figure 4-11. Tape Speed Selection Examples

WAN-0084

EXAMPLE FOR:

Tape Unit A = 9-Track 800 BPI
Tape Unit B = 7-Track 800/556 BPI
Tape Unit C = 7-Track 556/200 BPI
Tape Unit D = 7-Track 800/200 BPI

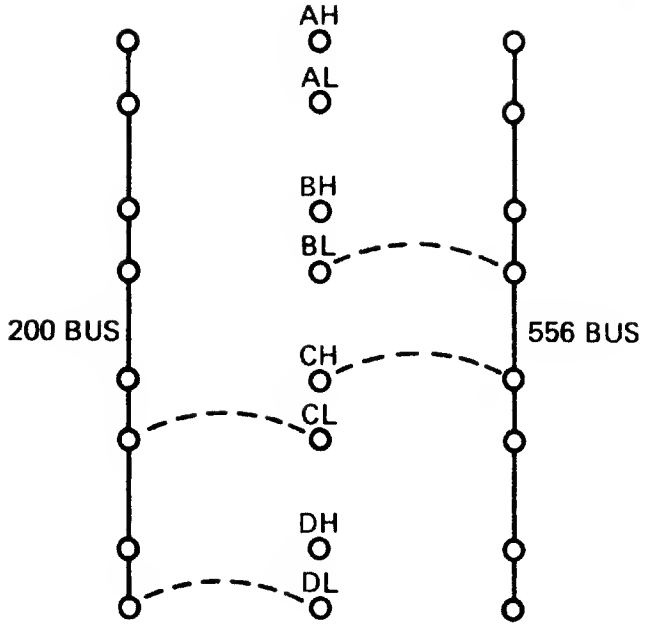


Figure 4-12. Density Selection Wiring Example

4.7.3 SINGLE/DUAL STACK HEAD SELECTION

The Formatter is configured so that if no jumpers are used in the SS/DS Head Selection Field, the Dual-Stack (Read-After-Write) configuration is in effect. Jumpers must be used only for Tape Units (A, B, C, or D) that are single-stack head units. The SS/DS Head Selection Field is located on the Control Board assembly number 201659 near chip position G7. Bus 603 must be jumpered to points A, B, C, or D for single-stack Tape Units correspondingly designated A, B, C, or D. If Tape Units are equipped to report Single-Stack Status, then E617 may be jumpered to E603 for Tape Unit control of Single-Stack logic.

4.7.4 BCD 10 TO ZERO CONVERTER (READ)

The Formatter is configured to convert BCD 10 (Octal 12) to zero when reading 7-track tapes in the even parity mode if no jumper is inserted between E604 and E605 on the Control Board assembly. Insertion of the jumper from E604 to E605 causes the BCD 10 to be read without conversion to the Controller. The BCD 10 code is equivalent to a 1 bit on lines $\overline{R4}$ and $\overline{R6}$, and a 0 bit on lines $\overline{R2}$, $\overline{R3}$, $\overline{R5}$, $\overline{R7}$ and $\overline{RP}$.

4.7.5 ZERO TO BCD 10 CONVERTER (WRITE)

The all-zeros code is automatically converted to the BCD 10 code when writing on a 7-track Tape Unit in the even parity mode if there is no jumper between E623 and E624; thus, there must be at least one track with a 1 bit in it to generate a Read Data Strobe pulse when reading back.

NOTE

The BCD 10 code is forbidden as an industry standard when writing on 7-track tapes in the even-parity mode unless the program is constructed to handle the following items:

- Conversion of BCD 10 to zero upon writing (no jumper between E604 and E605).
- Conversion of zero to BCD 10 upon reading (with jumper between E623 and E624).

4.7.6 7-TRACK FILE MARK CODE WRITE/READ ON 9-TRACK TAPE UNIT

The Formatter is configured to Write/Read normal File Marks (Octal 23) with 9-track Tape Units when no jumper is installed between E608 and E609 on the Control Board assembly. With the jumper installed, a dummy 7-track code File Mark (Octal 17) is written and checked to provide compatibility with existing computer software.

4.7.7 NO PARITY ERROR FOR FILE MARKS

The Formatter is configured to indicate a parity error when reading a 7-track File Mark in the odd parity mode, or when reading a dummy 7-track File Mark on a 9-track Tape Unit (with no jumper installed between E606 and E607 on the Control Board assembly). With the jumper installed, the parity error indication is disabled.

4.7.8 REWIND INTERRUPT

The Formatter is configured to set CBUSY when the Rewind command is issued if no jumper is present between E601 and E602 on the Control Board assembly. CBUSY resets when the Rewind operation is completed. This provides a signal to the Controller to indicate the next command can be accepted. If jumper E601 to E602 is present, CBUSY does not set for a Rewind command.

4.7.9 FORMATTER ADDRESS SELECT

The Formatter is configured to always be selected if no jumper is placed in the Formatter Address Select; therefore, if a single Formatter is used, no jumper needs to be used. Table 4-5 lists the jumper connection required for various addressing schemes.

TABLE 4-5. Formatter Address Selection

Formatter Address	Jumper Configuration	Remarks
None	None	Formatter always selected
0	E611 to E612	$\overline{\text{FAD1}}$ signal High
1	E610 to E612	$\overline{\text{FAD1}}$ signal Low
NRZI	E616 to E612	$\overline{\text{NRZ}}$ signal Low (Tape Unit Selects Formatter)
Hi Density	E632 to E612 and E631 to E629 (remove E629 to E630)	$\overline{\text{Hi Density}}$ signal High (Controller Selects Formatter and Tape Unit with Density Line)
NOTE: Only one of these jumper configurations may be installed.		

4.7.10 DISABLE MANUAL CONTROL OF PARITY AND DENSITY

To disable manual control so that Controller signals always control parity and density, establish the following jumper configurations on the Control Board assembly:

A. Remove the jumper between E621 and E622.
B. Add jumpers from E618 and E619 to E620.
C. Add a jumper between E629 and E630.

4.7.11 DISABLE REMOTE CONTROL OF DENSITY

To allow manual or remote control over parity selection while allowing density selection to be controlled from only the front panel density switch, the Controller must supply a Low (gnd) signal for Hi Density on pin 77 and the Main Board assembly must have the following jumper configuration:

A. Jumpers from E618 and E619 to E620.
B. No jumper between E621 and E622.

4.7.12 NORMAL REMOTE/MANUAL CONTROL OF DENSITY AND PARITY

The Normal Remote/Manual mode of operation is most commonly used to control density and parity. This mode is established by the following jumper configurations on the Control Board assembly:

A. Remove jumpers from E618 and E619 to E620.
B. Connect jumpers between E619 and E620, E621 and E622, and E629 and E630.
C. Connect a jumper between E625 and E626 (only if automatic selection of the odd parity mode is desired when a 9-track Tape Unit is selected).

4.7.12.1 Remote Mode. In Remote mode, the HI DENSITY and GEN ODD PARITY signals from the Controller control the 7-track density and the 7-track or 9-track parity selection, respectively.

4.7.12.2 Manual Mode. In Manual mode, the DENSITY and PARITY switches on the OCP of the Formatter control 7-track density and parity, respectively.

4.7.13 JUMPER FUNCTIONS SUMMARY

Table 4-6 lists a summary of all jumpers, their functions, and the related logic schematic drawing.

TABLE 4-6. Jumper Functions

Jumper	Function	Logic Schematic
E601 to E602	No Interrupt for Rewind	5
E603 to A,B,C,D	Single-Stack Head Designation	5
E603 to E617	Tape Unit Selection of Single-Stack Logic	5
E604 to E605	Disable BCD 10 to Zero Conversion (Read)	8
E606 to E607	Disable Parity Error for File Mark	11
E608 to E609	Enable Write 7-Track File Mark Code in 9-Track Mode	7
E610 to E612	Enable Formatter Address ONE	13
E611 to E612	Enable Formatter Address ZERO	13
E615 to E612	Not Used	13
E616 to E612	Enable NRZ Selection of Formatter	13
E632 to E612	Enable HI DENSITY Selection of Formatter (Remote Density Select)	13
E613 to E614	Deleted if Dual Density (PE/NRZI) Formatter	12
E618, E619, E620, E621 and E622	(Ref. paragraphs 4.7.1 through 4.7.2)	12
E623 to E624	Disable Zero to BCD 10 Conversion (Write)	7
E625 to E626	Enable Automation Selection of ODD Parity for 9-Track	12
E629 to E631	Enable Remote Density Select	12
E501 to E503	0.150-inch (3.81mm) R/W Head Gap	3
E502 to E503	0.300-inch (7.62mm) R/W Head Gap	3

4.8 DELAY TIMES

The state flow diagrams (ref. figures 4-3 and 4-4) show three principal delay times:

A. Predelay

B. Postdelay

C. Halt Delay

4.8.1 PREDELAYS AND POSTDELAYS

The Predelays and Postdelays are used to erase portions of the IRG (when writing) or to erase tape. When reading, they are used to correctly position the tape under the head in the IRG so that the subsequent record can be either a Read or a Write operation.

4.8.2 HALT DELAY

The Halt delay is also used to erase part of the IRG when writing and provides sufficient time to ensure that the Tape Unit is completely stopped (after the motion signal is terminated).

4.8.3 DELAY TIME FACTORS

The following factors determine the times of the various delays:

A. Number of tracks (7 or 9)
B. Tape speed
C. Number of heads (single or dual)
D. Motion direction (forward or reverse)
E. Starting point (beginning of tape or not)
F. Type of command (Write or Read)
G. Type of mode (Edit or not)

4.9 POWER SUPPLY

The power supply (WANGCO PN 201581) is an integral assembly of the Formatter and furnishes all operating voltages required by the Formatter electronics. Selectable taps on the primary winding of the transformer enable operation from any of the following 48 to 62 Hz line voltages: 100V, 110V, 115V, 120V, 125V, 200V, 220V, 230V, 240V, or 250V, at 160W. Application of AC input power is controlled by a switch/indicator pushbutton (S101) mounted on the OCP at the front panel of the Formatter. The power supply provides the following outputs:

A. Unregulated, +13V (nominal)
B. Regulated, +5V, 9A

The regulated +5V circuitry includes foldback current limiting, overvoltage protection, and reverse voltage protection. Fuses provide additional protection against overload.

4.9.1 PHYSICAL DESCRIPTION

The power supply consists of four major assemblies which support various subassemblies and components:

A. Chassis
B. Back panel
C. Side panel
D. Circuit board

The chassis contains the power transformer, high-current rectifiers, a filter capacitor, heatsink-mounted power transistors, an SCR, the circuit board, and terminal block TB1.

Terminal block TB201, and fuses F201 and F202 are mounted in the back panel. AC line-power input is terminated at TB201.

The side panel supports a blower fan and terminal block TB202. This panel is mechanically interconnected to the chassis and back panel. AC power is routed from TB201 via F201 to TB202, where it is distributed to power switch S101 (on Formatter front panel), blower fan B101, and power transformer T1 via TB1.

TB202 terminates a voltage from circuit board connection J4/P4 which is routed to the power-on indicator lamp in switch/indicator S101.

4.9.2 CIRCUITRY DESCRIPTION

The power supply circuitry provides regulated and unregulated voltages, and various protective circuits.

4.9.2.1 Voltage Outputs. DC power for the Formatter is developed by a standard half-wave rectifier/capacitive filter circuit. The filtered voltage is regulated by the series-pass transistor of a complementary pair of power transistors, Q1 and Q2 (on the chassis). The base of Q1 is driven by integrated circuit (IC) regulator U1, and associated components, which establish the reference voltage. This regulator can hold a given voltage setting within $\pm 1\%$ against variations in line voltage, load, and ambient temperature. The regulated voltage output of the power supply is maintained within a tolerance of $\pm 5\%$ which includes line voltage-load-temperature variations,

component aging, and a 2% setting accuracy. The +5V regulated output is terminated at two locations on the circuit board:

A. Pin 5 of J202 where it is distributed to the Formatter electronics via P202 and associated wiring.
B. Pin 1 of J4 where it is distributed, via TB202, to the power-on indicator lamp in S101 on the OCP at the Formatter front panel.

The filtered, but unregulated +13V output of the power supply is terminated on the circuit board at pin 3 of J202 where it is distributed to the Formatter electronics via P202 and associated wiring. This voltage ranges from +13V (high line voltage, minimum load) to +9V (low line voltage, maximum load). The power supply ground is terminated on the circuit board at pins 1 and 2 of J202, and at pin 3 of J4.

4.9.2.2 Short Circuit Protection. This circuitry is of the foldback, current-limiting type; therefore, a short circuit at the output can be safely sustained for an indefinite time. Tolerance on the foldback knee ensures that regulation is maintained with load currents up to 9 amperes (A); however, load currents exceeding 9A can overstress the power supply.

4.9.2.3 Overvoltage and Reverse Voltage Protection. Any overvoltage condition is detected by transistors Q1 and Q2 (on the circuit board) and associated components. Overvoltage applies forward bias to the emitter-base junction of Q1. The resulting current drive from Q1 attains unity gain in emitter-follower Q2 which fires SCR1. SCR1 then short circuits the unregulated voltage to ground. DC fuse F202 then blows and removes the regulator input voltage from U1. Protection against overvoltage, caused by malfunction of power transistors Q1 and Q2 (on the chassis) or IC regulator U1, is thus ensured. High-current diode CR3 (on the circuit board), which is connected between the unregulated input and regulated output, clamps externally applied overvoltages and produces up to 3A of steady-state current. Protection against reverse voltage, externally applied on the regulated +5V line, is provided by diode CR7 (on the circuit board).

SECTION 5

MAINTENANCE AND TROUBLESHOOTING

5.1 GENERAL

This section provides brief maintenance recommendations for the WANGCO Model 511 NRZI Formatter.

5.2 MAINTENANCE

Maintenance of the Formatter is based primarily on understanding the theory of operation (Section 4) coupled with the use of the logic schematics and engineering drawings.

Removal and installation of Formatter assemblies, components, and detail parts for maintenance purposes is straightforward; however, some general notes and precautions are provided in the following paragraphs.

WARNING

PRIOR TO REMOVAL OR INSTALLATION OF ANY FORMATTER POWER SUPPLY PARTS, ALWAYS DISCONNECT POWER CABLE FROM SOURCE.

The Formatter requires no adjustments. Additionally, there are no air filters to clean; however, the fan and the areas through which the air passes should be checked periodically to avoid restrictions.

5.3 GENERAL TROUBLESHOOTING

With the top cover removed, all Formatter components are exposed for in-place troubleshooting. Accessibility is shown in Figure 5-1.

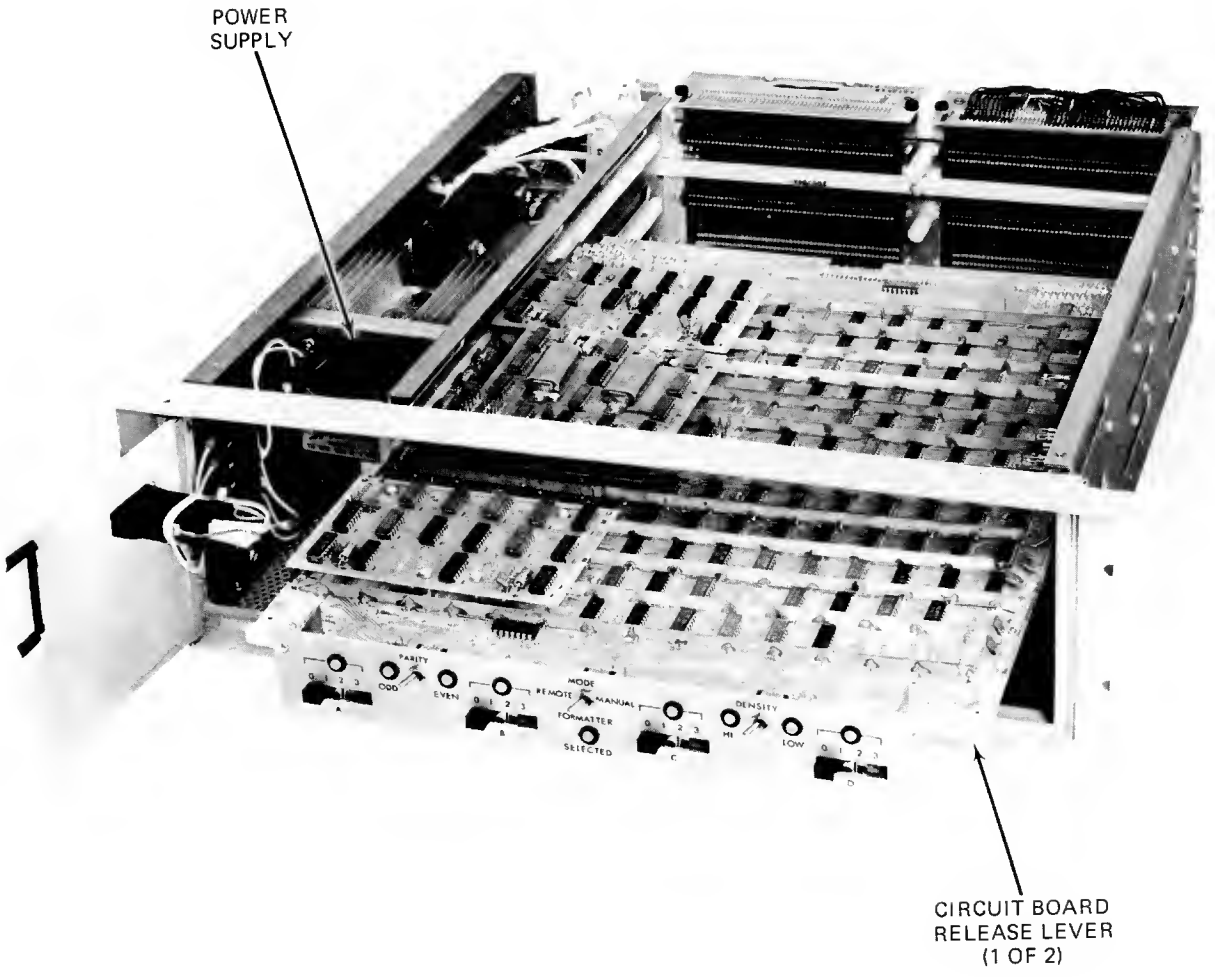


Figure 5-1. Formatter with Top Cover Removed and Circuit Boards Partially Extended

5.3.1 CIRCUIT BOARD REMOVAL

The NRZI Control board is removed through the front by using the nylon card extractors attached to either side of the board. The other boards (CRC Generator, Delay Counter, and Clock Generator) are plugged into the major assembly board and secured with 4-40 screws.

When reinserting any circuit board, make sure it is seated firmly into the appropriate connector.

CAUTION

POWER SHOULD BE TURNED OFF PRIOR TO REMOVING OR REPLACING ANY CIRCUIT BOARD.

5.3.2 REFERENCE DESIGNATIONS

All components are clearly identified, and an alphanumeric grid system is used as reference designations to identify chip locations. The alphabet characters read from left to right (as viewed from the front) and the numerical characters read from front to back as shown in Figure 5-2.

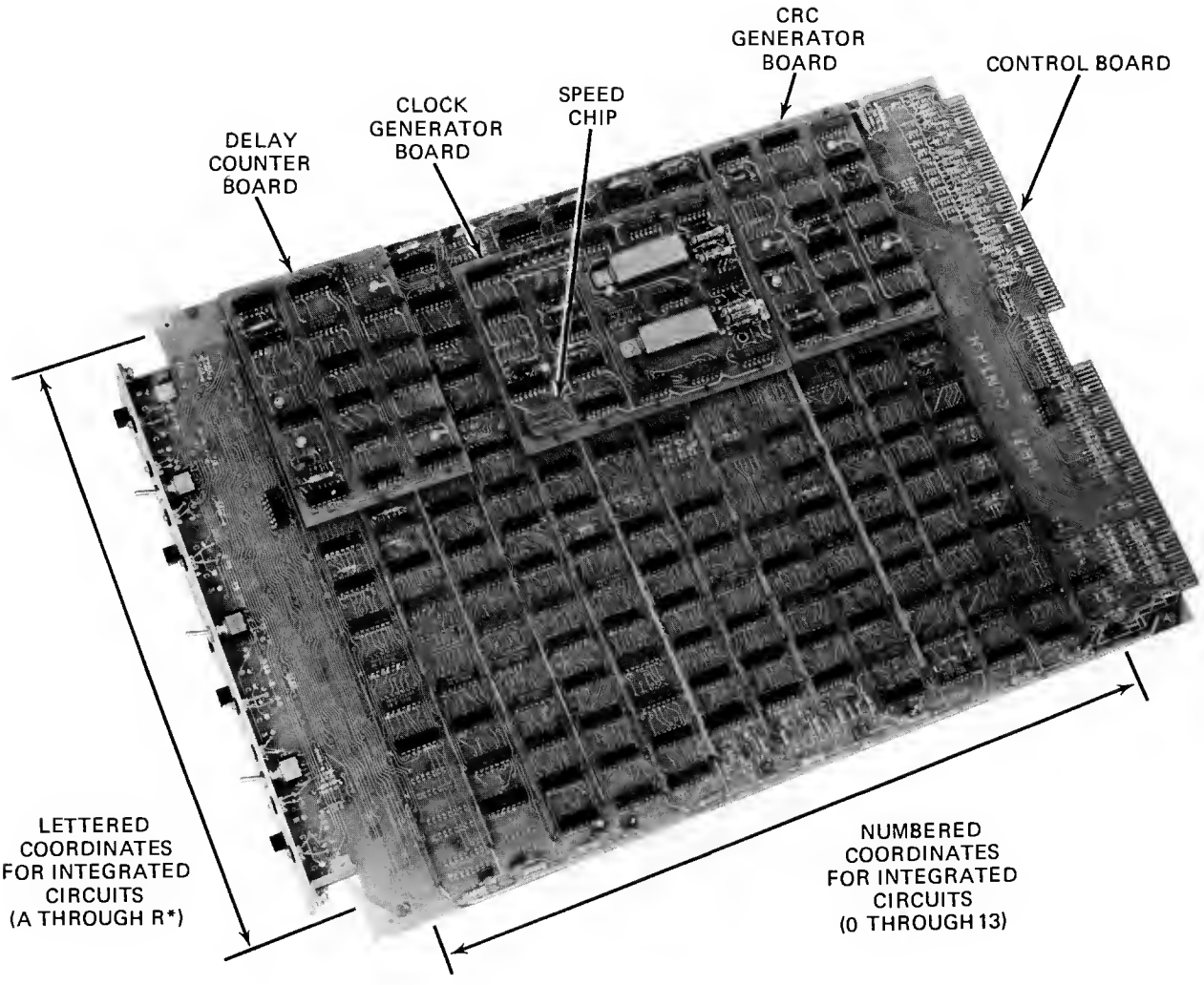
5.3.3 FUSES

Always ensure that fuse replacements are the same type, voltage, and current ratings as those being removed. This can normally be verified by the placard located adjacent to the fuse receptacles (ref. figure 2-1); however, the following caution must be observed.

CAUTION

SINCE THE SOURCE-POWER CONFIGURATION MAY HAVE BEEN CHANGED IN THE FIELD WITHOUT CHANGING THE PLACARD, CHECK THE POWER SUPPLY CONFIGURATION AND APPROPRIATE FUSE AGAINST THE POWER SUPPLY SCHEMATIC IN APPENDIX C IF ANY REPEATED POWER SUPPLY PROBLEM (SUCH AS REPEATED FUSE FAILURES) OCCURS.

If a fuse fails, WANGCO recommends the cause of fuse failure be determined and corrected before replacing the failed fuse.



NOTES:

*1. Letters I, O, and Q are not used.
2. Discrete components on CRC Generator Board are in 300 series.
3. Discrete components on Clock Generator Board are in 400 series.
4. Discrete components on Delay Counter Board are in 500 series.
5. Discrete components on Control Board are in 600 series except for Tape Unit termination resistors which are in 700 series, and front panel components (lamps and switches) which are in unit series (e.g. S1 and DS1).

Figure 5-2. Formatter Circuit Boards and Component Locations (Except Power Supply)

SECTION 6

LOGIC DATA

6.1 GENERAL

This section contains all data essential to the logic functions of the WANGCO Model 511 NRZI Formatter as described in this manual. The information is presented in the following sequence:

A. Glossary of Terms
B. Integrated Circuit Reference Data
C. Description of Logic and Symbols

6.2 GLOSSARY OF TERMS

Table 6-1 lists a complete and comprehensive glossary of terms for the NRZI Formatter and defines, in alphabetical order, the various abbreviations, acronyms, and other mnemonics used throughout this manual.

6.3 INTEGRATED CIRCUIT DATA

Table 6-2 lists integrated circuit chip reference designations and corresponding WANGCO part numbers.

Table 6-3 lists the applicable WANGCO part number of each integrated circuit used on the NRZI Formatter, together with the manufacturer's technical reference data.

6.4 DESCRIPTION OF LOGIC AND SYMBOLS

DTL and TTL logic of the typical inverting type (NAND–NOR) rather than (AND–OR) is used, though some AND–OR elements are employed. Although the same device may be used to implement both the NAND and the NOR function, the symbols shown on the logic schematics correspond to the particular functional operation.

TABLE 6-1. NRZI Formatter Glossary of Terms (continued)

Term	Definition
ADDR	Formatter Addressed
AS1 & AS2	Activity Sense 1 & 2
BOT	Beginning of Tape
BSR	Backspace Record
B0–B7	Write Data Input from Computer Adapter
CBP, CB0–CB7	Write Data Storage Buffer
CC 1, 2, 4	Character Counter 1, 2, 4
CD	Core Dump
CK WD CNT	Check Word Count
CLK	180 KHz Clock to Computer Adapter
CLKS	State Counter Clock
CLR	Clear Command Storage
CRC P, 0–7	CRCC Register
DBY	Data Busy
DATA FLAG	Data Transfer Request Flag
DDI	Data Density Indicator
DDS	Data Density Select
DFCL	Data Flag Clock
DGATE	Read Data Gate
DP, D0–7	Read Buffer Outputs
DS	Data Strobe
DS0	Rest State of State Counter
DS1–DS7	State Counter Inputs
EBCC	Enable Blank Character Counter
EDIT	Edit Mode
ENCRC	Enable CRCC
END	End Delay Period
EOT	End of Tape
EOTS	End of Tape Status
EWDR	Enable Write Data Requests
EXITS3	Exit State 3
EXTRESET	External Reset from Computer Adapter
EXTRJCT	External Reject Command from Computer Adapter

TABLE 6-1. NRZI Formatter Glossary of Terms (continued)

Term	Definition
FAD1	Formatter Address
FM	File Mark Status
FM DET	File Mark Code Detected
FPT	File Protect
F200	200 BPI Selected
F556	556 BPI Selected
F800	800 BPI Selected
GEN ODD PARITY	Generate Odd Parity
HALT	Halt Data Transfer Requests
HI DENSITY	Select Density
LDP	Load Point
LER	LRCC Error
LP, L0–7	LRCC Register
M1–M128	Delay Counter Outputs
OFFC	Offline Command to Tape Unit
OFLC	Offline Command Storage
ON LINE	Tape Unit is On Line
OVW	Overwrite to Tape Unit (Same as Edit)
PARITYER	Parity Error
POR	Power On Reset
RCAS	Read Clock Activity Sense
RCC	Read Command
RDP–RD7	Read Data from Tape Unit
RDS	Read Data Strobe
RDY	Tape Unit Ready
REJECT	Command Rejected Status
REW	Rewind Command Storage
REWINDING	Tape Unit Rewinding Status
RJCT	Command Rejected Pulse
RSTCNTR	Reset Delay Counter

TABLE 6-1. NRZI Formatter Glossary of Terms (continued)

Term	Definition
RST STOP	Reset STOP Flip-Flop
RSTR	Read Strobe from Formatter to Computer Adapter
RSTROBE	Read Strobe from Tape Unit to Computer Adapter
RW	Rewind Command Storage
RWC	Rewind Command to Tape Unit
RWDG	Rewinding Status
RP, R0–7	Read Data Bits P, 0–7 to Computer Adapter
SELECT A–D	Tape Unit Select Lines
SETCLR	Clear Command from Computer Adapter
SETFSR	Forward Space Record from Computer Adapter
SETGAP	Erase Command from Computer Adapter
SETOFL	Offline Command from Computer Adapter
SET PE	Set Parity Error
SETRCC	Read Command from Computer Adapter
SETREV	Reverse Command from Computer Adapter
SETREW	Rewind Command from Computer Adapter
SETRJCT	Command Requiring Write Current
SETWCC	Write Command from Computer Adapter
SETWFM	Write File Mark Command from Computer Adapter
SFC	Synchronous Forward Command to Tape Unit
SINGLE	Single Gap Head Status from Tape Unit
SPDCLK	Speed Clock
SRC	Synchronous Reverse Command to Tape Unit
SRS	System Reset Pulse
SS	Single Stack Head
STOP	STOP Delay Counter
STOPSPACE	Stop Spacing (Forward or Reverse)
STROBEC	Command Strobe
SWS	Set Write Status
S1–7	State Counter
S1*,S2*	Tape Unit Select Lines from Computer Adapter
S1, S2, S4, S8, S16	Encoded Outputs from Speed Chip

TABLE 6-1. NRZI Formatter Glossary of Terms (concluded)

Term	Definition
THR1	Threshold 1 (High)
THR2	Threshold 2 (Low)
TMER	Data Transfer Timing Error Status
TM1, TM2, TM4	Speed Clock divide by 5 Flip-Flops
TRD	Test Read
TU0 -TU3	Decoded Tape Unit Select Lines
VLD	Valid Pulse
VPE	Vertical Parity Error
WARS	Write Amplifiers Reset
WCC	Write Command
WCLK	Write Clock
WCLP	Write Clock Pulse
WDP--WD7	Write Data to Tape Unit
WDS	Write Data Strobe
WFM	Write File Mark
W/RACK	Write/Read Acknowledge
WRMSB	Write Most Significant Byte
WRP	Write Precede Pulse
1st CH	1st Character
2nd CH	2nd Character
7TRK	7 Track Tape Unit
7EV	7 Track - Even Parity Mode
7ODD	7 Track - Odd Parity Mode
9TRK	9 Track Tape Unit

TABLE 6-2. Integrated Circuit Reference Designation Versus WANGCO Part Number (continued)

Reference Designation①	Wangco Integrated Circuit Part No.
A1	100085
A2	100085
A3	Spare
A4	100332
A5	Spare
A6	100085
A7	100084
A8	100331
A9	100336
A10	100336
A11	100329
A12	100426
B1	100329
B2	101014
B3	101014
B4	100336
B5	100085
B6	N/A
B7	100085
B8	101014
B9	101014
B10	100426
B11	101014
B12	100339
C1	②
C2	100349
C3	100346
C4	100336
C5	100085
C6	100085
C7	N/A
C8	N/A
C9	N/A
C10	③
C11	100341
C12	100339
D1	100349
D2	100349
D3	100085
D4	100349
D5	④
D6	100329
D7	101014
D8	100329
D9	100347
D10	100336
D11	100341
D12	100339
E1	⑤
E2	100085
E3	100346
E4	100335
E5	100084
E6	100085
E7	N/A
E8	N/A
E9	N/A
E10	⑥
E11	100341
E12	100339
F0	100336
F1	100348
F2	100107
F3	100329
F4	100336
F5	⑦
F6	100332
F7	100346
F8	100346
F9	101014
F10	100336
F11	100341
F12	100339
G1	100335
G2	100331
G3	100329
G4	100085
G5	100084
G6	100085
G7	100084
G8	N/A
G9	N/A
G10	100427
G11	100336
G12	100336
H1	100107
H2	100329
H3	100336
H4	100107
H5	100329
H6	Spare
H7	Spare
H8	100347
H9	100331
H10	100084
H11	100340
H12	100340
J1	100085
J2	100085
J3	100085
J4	100107
J5	100339
J6	100085
J7	100336
J8	N/A
J9	100336
J10	100085
J11	100341
J12	100341
K1	101014
K2	Spare
K3	100085
K4	100085
K5	101014
K6	100329
K7	100107
K8	100340

TABLE 6-2. Integrated Circuit Reference Designation
Versus WANGCO Part Number (concluded)

Reference Designation ①	Wangco Integrated Circuit Part No.
K9	100329
K10	100085
K11	100341
K12	100341
L1	101014
L2	101014
L3	101014
L4	100085
L5	100107
L6	100339
L7	100425
L8	100085
L9	100085
L10	100087
L11	100087
L12	100087
M1	100348
M2	100329
M3	101014
M4	100332
M5	100085
M6	100107
M7	100335
M8	100340
M9	100336
M10	100336
M11	100336
M12	100336
N1	Spare
N2	100085
N3	100084
N4	100348
N5	100085
N6	100329
N7	100348
N8	100332
N9	100341
N10	100340
N11	100340
N12	Spare
P1	Spare
P2	N/A
P3	100349
P4	100329
P5	100339
P6	100339
P7	100339
P8	100348
P9	101014
P10	101014
P11	101014
P12	101014
P13	100327
R1	Spare
R2	Spare
R3	100329
R4	100085
R5	100085
R6	N/A
R7	N/A
R8	N/A
R9	100339
R10	100427
R11	100335
R12	100084
U1	100327

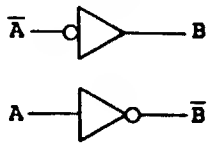
NOTES

① Reference designations used on Logic Diagrams, Assembly Drawings, and Material Lists.
② Delay Counter to Control Board Connector (1 of 2; see E1).
③ CRC Generator to Control Board Connector (1 of 2; see E10).
④ Clock Generator to Control Board Connector.
⑤ Delay Counter to Control Board Connector (1 of 2; see C1).
⑥ CRC Generator to Control Board Connector (1 of 2; see C10).
⑦ Speed Chip P/N determined by Tape Unit Speed.

TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100084
COMMERCIAL EQUIVALENT: 15836N
TITLE: HEX INVERTER (DTL)

SYMBOL:

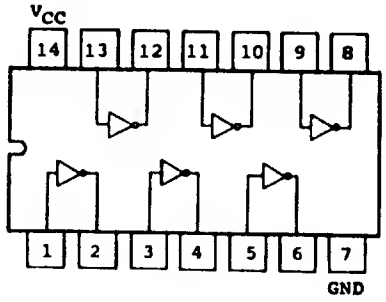


EQUATION:

$B = \overline{A}$

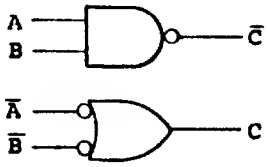
$\overline{B} = A$

PACKAGE:



WANGCO P/N: 100085
COMMERCIAL EQUIVALENT: 15846N
TITLE: QUAD 2-INPUT NAND (DTL)

SYMBOL:

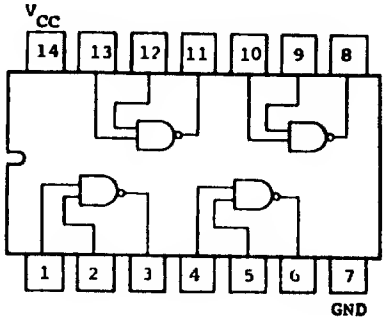


EQUATION:

$\overline{C} = A \cdot B$

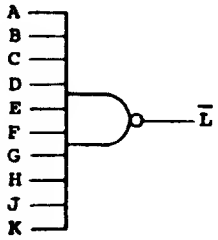
$C = \overline{A} + \overline{B}$

PACKAGE:



WANGCO P/N: 100087
COMMERCIAL EQUIVALENT: 151804N
TITLE: 10-INPUT NAND (DTL)

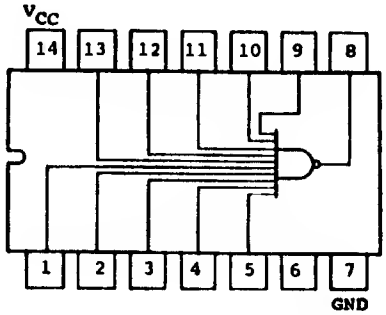
SYMBOL:



EQUATION:

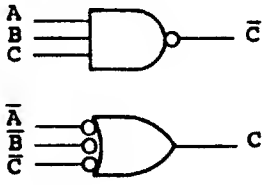
$\overline{L} = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot J \cdot K$

PACKAGE:



WANGCO P/N: 100107
COMMERCIAL EQUIVALENT: 15862N
TITLE: TRIPLE 3-INPUT NAND (DTL)

SYMBOL:



EQUATION:

$\overline{C} = A \cdot B \cdot C$

$C = \overline{A} + \overline{B} + \overline{C}$

PACKAGE:

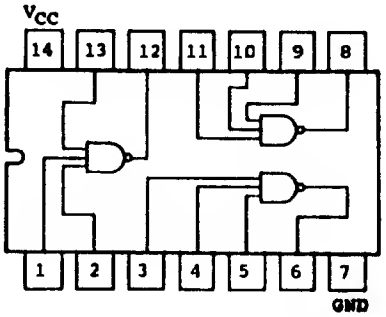


TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N 100327
COMMERCIAL EQUIVALENT: 7407N
TITLE: HEX BUFFER (TTL) (OC)

SYMBOL:

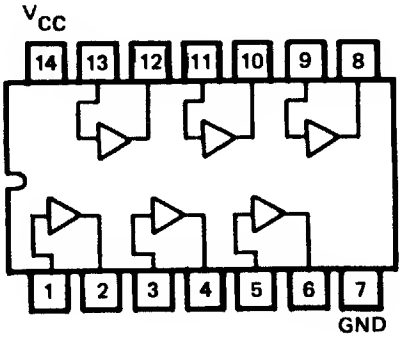
OR

EQUATION:

$\overline{B}=\overline{A}$

$B=A$

PACKAGE:



WANGCO P/N: 100329
COMMERCIAL EQUIVALENT: 7402N
TITLE: QUAD 2-INPUT NOR (TTL)

SYMBOL:

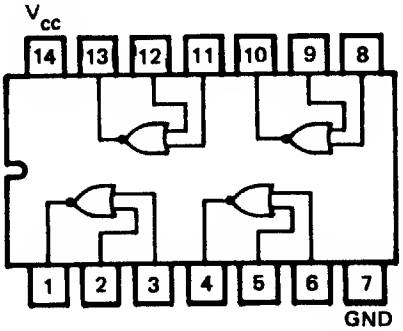
OR

EQUATION:

$\overline{C} = A + B$

$C = \overline{A} \cdot \overline{B}$

PACKAGE:



WANGCO P/N: 100331
COMMERCIAL EQUIVALENT: 7406N
TITLE: HEX INVERTER BUFFER (TTL) (OC)

SYMBOL:

OR

EQUATION:

$B=\overline{A}$

$\overline{B}=A$

PACKAGE:

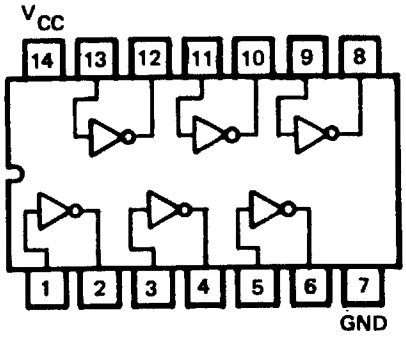
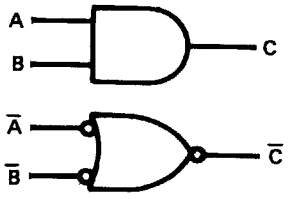


TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100332
COMMERCIAL EQUIVALENT: 7408N
TITLE: QUAD 2-INPUT AND (TTL)

SYMBOL:



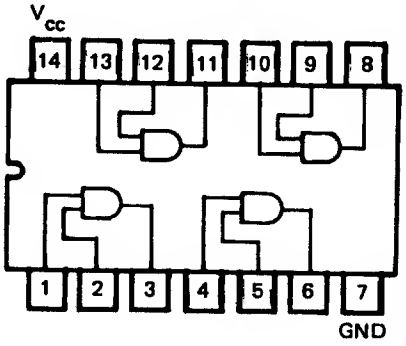
EQUATION:

$C = A \cdot B$

OR

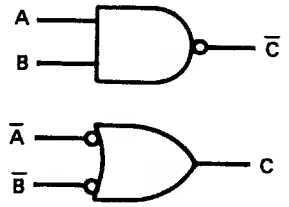
$\overline{C} = \overline{A} + \overline{B}$

PACKAGE:



WANGCO P/N: 100335
COMMERCIAL EQUIVALENT: 7437N
TITLE: QUAD 2-INPUT NAND BUFFER (TTL)

SYMBOL:



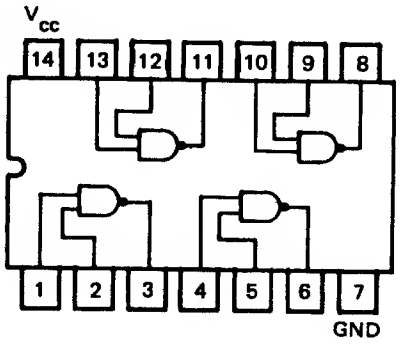
EQUATION:

$\overline{C} = A \cdot B$

OR

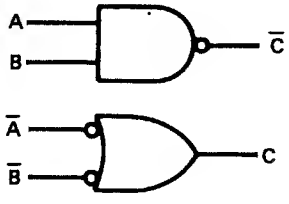
$C = \overline{A} + \overline{B}$

PACKAGE:



WANGCO P/N: 100336
COMMERCIAL EQUIVALENT: 7438N
TITLE: QUAD 2-INPUT NAND BUFFER (OC) (TTL)

SYMBOL:



EQUATION:

$\overline{C} = A \cdot B$

OR

$C = \overline{A} + \overline{B}$

PACKAGE:

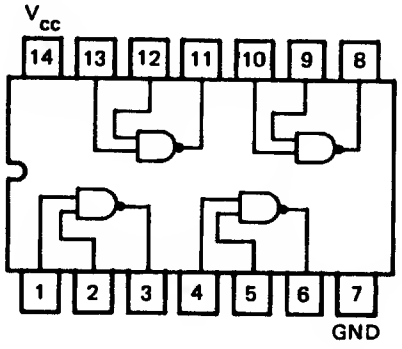
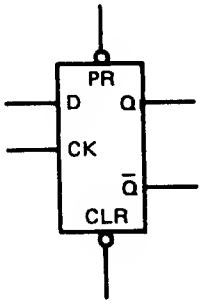


TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100339
COMMERCIAL EQUIVALENT: 7474N
TITLE: DUAL D-TYPE FLIP-FLOP (TTL)

SYMBOL:



FUNCTION TABLE:

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

* THIS CONFIGURATION IS NONSTABLE; THAT IS, IT WILL NOT PERSIST WHEN PRESET AND CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.

PACKAGE:

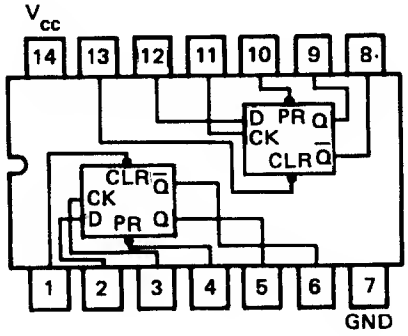
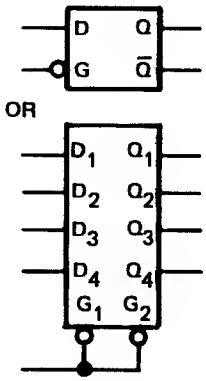


TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100340
COMMERCIAL EQUIVALENT: 7475N
TITLE: QUAD BI-STABLE LATCH (TTL)

SYMBOL:

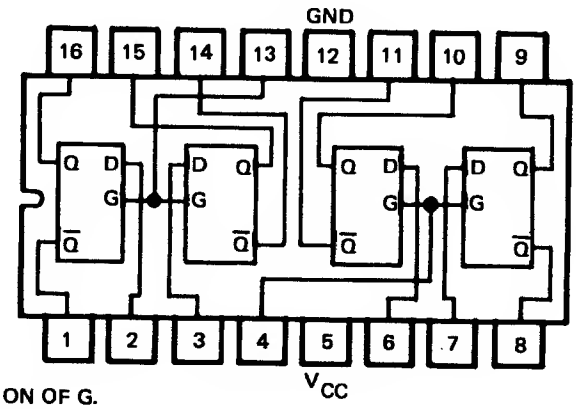


FUNCTION TABLE:
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = HIGH LEVEL
L = LOW LEVEL
X = IRRELEVANT
Q_0 = THE LEVEL OF Q BEFORE THE HIGH TO LOW TRANSITION OF G.

PACKAGE:



DESCRIPTION: INFORMATION PRESENT AT A DATA (D) INPUT ARE TRANSFERRED TO THE Q OUTPUT WHEN THE ENABLE (G) IS HIGH AND THE Q OUTPUT WILL FOLLOW THE DATA INPUT AS LONG AS THE ENABLE REMAINS HIGH. WHEN THE ENABLE GOES LOW, THE INFORMATION (THAT WAS PRESENT AT THE DATA INPUT AT THE TIME THE TRANSITION OCCURRED) IS RETAINED AT THE Q OUTPUT UNTIL THE ENABLE IS PERMITTED TO GO HIGH.

WANGCO P/N: 100341
COMMERCIAL EQUIVALENT: 7486N
TITLE: QUAD 2-INPUT EXCLUSIVE OR GATES

SYMBOL:

EQUATION:

$C = A \oplus B$

OR

$C = A\bar{B} + \bar{A}B$

PACKAGE:

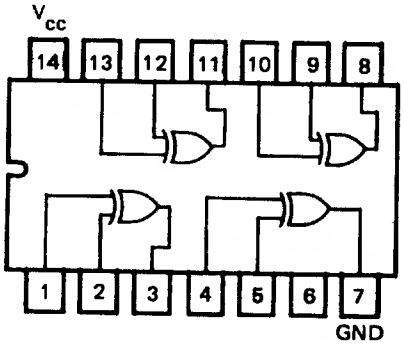
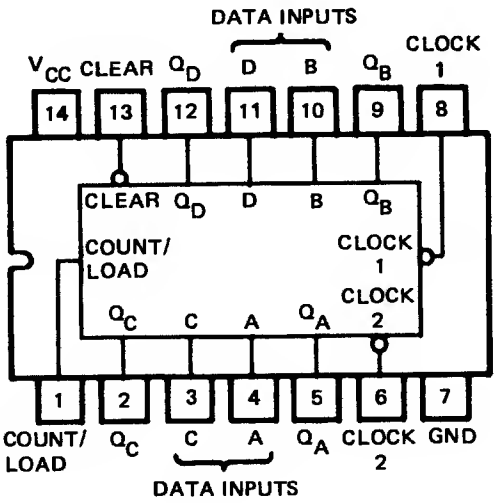


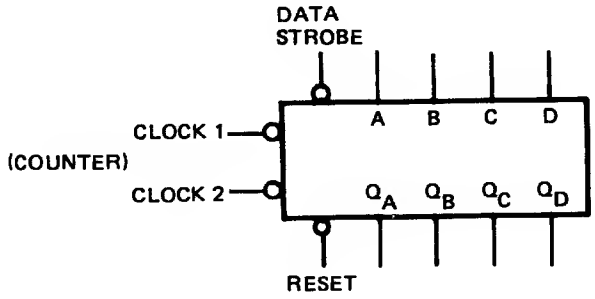
TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100346
COMMERCIAL EQUIVALENT: 8291B
TITLE: HI-SPEED BINARY COUNTER (TTL)

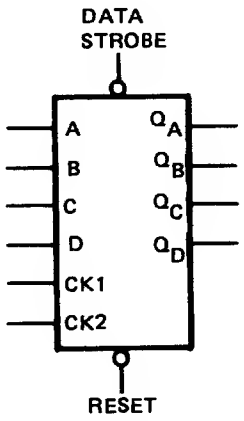
PACKAGE:



SYMBOL:



OR



BINARY				
INPUT	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

DESCRIPTION

THIS HIGH-SPEED MONOLITHIC COUNTER CONSISTS OF FOUR D-C COUPLED, MASTER-SLAVE FLIP-FLOPS WHICH ARE INTERNALLY INTERCONNECTED TO PROVIDE A DIVIDE-BY-TWO AND A DIVIDE-BY-EIGHT COUNTER. THE COUNTER IS FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAY BE PRESET TO ANY STATE BY PLACING A LOW ON THE COUNT/LOAD INPUT AND ENTERING THE DESIRED DATA AT THE DATA INPUTS. THE OUTPUTS WILL CHANGE TO AGREE WITH THE DATA INPUTS INDEPENDENT OF THE STATE OF THE CLOCKS.

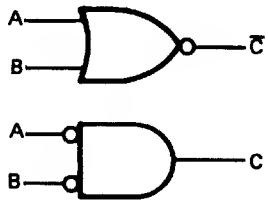
DURING THE COUNT OPERATION, TRANSFER OF INFORMATION TO THE OUTPUTS OCCURS ON THE NEGATIVE-GOING EDGE OF THE CLOCK PULSE. THE COUNTER FEATURES A DIRECT CLEAR WHICH, WHEN TAKEN LOW, SETS ALL OUTPUTS LOW REGARDLESS OF THE STATES OF THE CLOCKS.

THE COUNTER MAY ALSO BE USED AS A 4-BIT LATCH BY USING THE COUNT/LOAD INPUT AS THE STROBE AND ENTERING DATA AT THE DATA INPUTS. THE OUTPUTS WILL DIRECTLY FOLLOW THE DATA INPUTS WHEN THE COUNT/LOAD IS LOW, BUT WILL REMAIN UNCHANGED WHEN THE COUNT/LOAD IS HIGH AND THE CLOCK INPUTS ARE INACTIVE.

TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N 100347
COMMERCIAL EQUIVALENT: SP380A
TITLE: QUAD 2-INPUT NOR

SYMBOL:



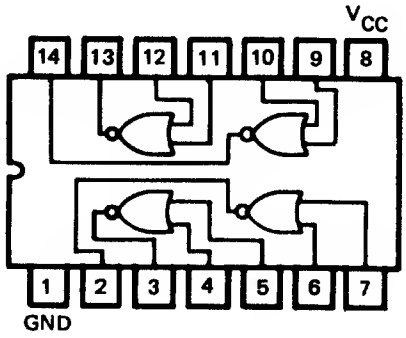
EQUATION:

$\overline{C}=A+B$

OR

$C=\overline{A}\cdot\overline{B}$

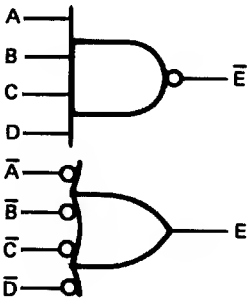
PACKAGE:



NOTE: THIS DEVICE IS SELECTED FOR ITS HIGH NOISE IMMUNITY PROPERTIES.

WANGCO P/N: 100348
COMMERCIAL EQUIVALENT: 930N
TITLE: DUAL 4-INPUT GATE WITH EXPANDER (DTL)

SYMBOL:



EQUATION:

$\overline{E}=A\cdot B\cdot C\cdot D$

OR

$E=\overline{A}+\overline{B}+\overline{C}+\overline{D}$

PACKAGE:

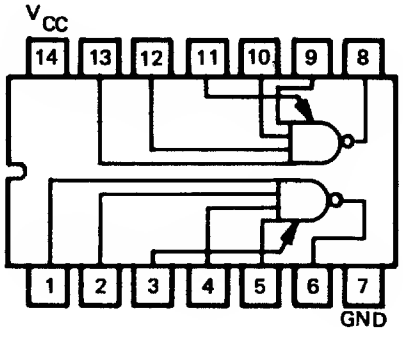
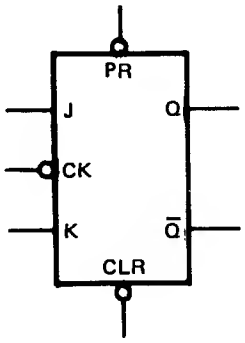


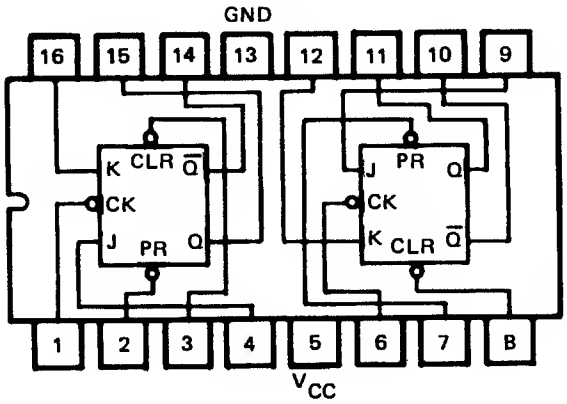
TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N: 100425
COMMERCIAL EQUIVALENT: 7476N
TITLE: DUAL J-K FF WITH PRESET AND CLEAR (TTL)

SYMBOL:



PACKAGE:



FUNCTION TABLE:

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

H = HIGH LEVEL (STEADY STATE)

L = LOW LEVEL (STEADY STATE)

X = IRRELEVANT

⎍ = HIGH LEVEL PULSE; DATA INPUTS SHOULD BE HELD CONSTANT WHILE CLOCK IS HIGH; DATA ARE TRANSFERRED TO OUTPUT ON THE FALLING EDGE OF THE PULSE

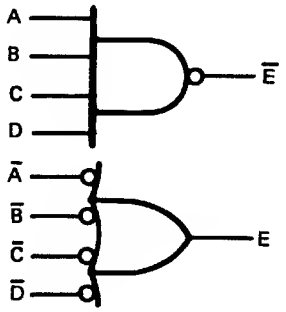
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

TOGGLE = EACH OUTPUT CHANGES TO THE COMPLEMENT OF ITS PREVIOUS LEVEL ON EACH ACTIVE TRANSITION (PULSE) OF THE CLOCK.

TABLE 6-3. Integrated Circuit Reference Data (continued)

WANGCO P/N 100426
COMMERCIAL EQUIVALENT: 7440N
TITLE: DUAL 4-INPUT NAND BUFFER (TTL)

SYMBOL:



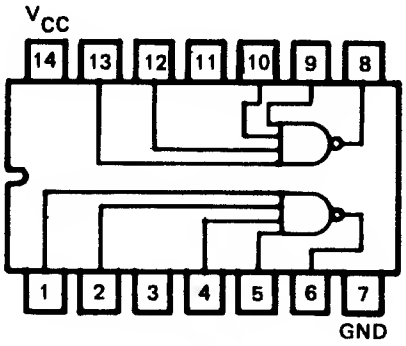
EQUATION:

$\overline{E} = A \cdot B \cdot C \cdot D$

OR

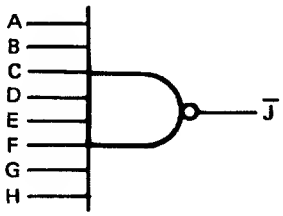
$E = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

PACKAGE:



WANGCO P/N: 100427
COMMERCIAL EQUIVALENT: 7430N
TITLE: 8-INPUT NAND GATE (TTL)

SYMBOL:



EQUATION:

$\overline{J} = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$

PACKAGE:

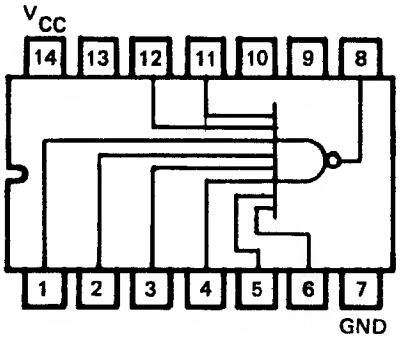
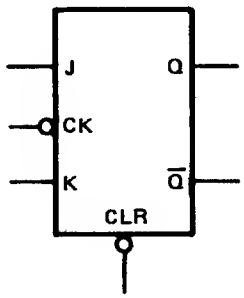


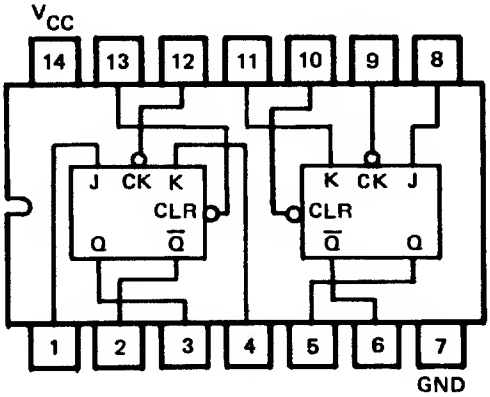
TABLE 6-3. Integrated Circuit Reference Data (concluded)

WANGCO P/N: 101014
COMMERCIAL EQUIVALENT: 74107N
TITLE: DUAL J-K M-S FLIP-FLOP (TTL)

SYMBOL:



PACKAGE:



FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
⎍ = HIGH LEVEL PULSE; DATA INPUTS SHOULD BE HELD CONSTANT WHILE CLOCK IS HIGH; DATA ARE TRANSFERRED TO OUTPUT ON THE FALLING EDGE OF THE PULSE.
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
TOGGLE = EACH OUTPUT CHANGES TO THE COMPLEMENT OF ITS PREVIOUS LEVEL ON EACH ACTIVE TRANSITION (PULSE) OF THE CLOCK.

In the logic schematics, the input/output lines to each device are shown for the TRUE (active) state of the function. A state indicator, shown as a small circle at the input or output of a device, signifies that, if that line is in the TRUE state, it is at a zero-Volt potential (low). Lack of a state indicator signifies that, if that line is in the TRUE state, it is at +5 Volts (high). Figure 6-1 shows an example of a logic symbol with definitions to provide clarification. The symbol depicts a logical NOR element which represents that output D at pin 4 is at +5 Volts if either input A at pin 1, B at pin 2, or C at pin 3 is at zero Volt. The numbers within the arrowheads indicate the source or destination of the related signal by logic schematic page number. An arrowhead placed adjacent to a signal line indicates a connection at that point. The logic schematic page number is enclosed by a hexagon in the lower right corner of each page.

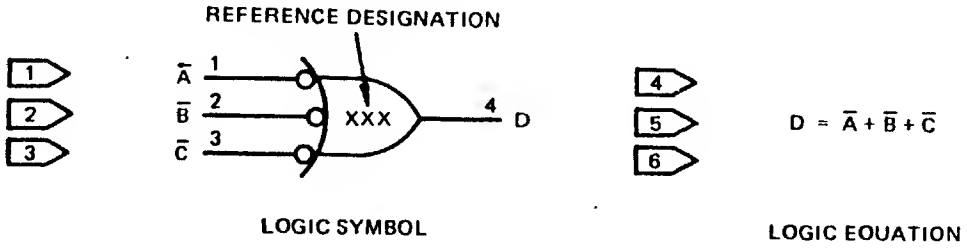


Figure 6-1. Logic Symbol Example

APPENDIX A

SPARE PARTS

A-1. RECOMMENDATIONS

The recommended spare parts for the WANGCO NRZI Formatter and Power Supply are listed in Master Spare Parts List 202176.

A-2. COMPONENT VARIANCE

For resistors, capacitors, small hardware, and other items not included in the list, equivalents in type, value, size, tolerance, and quality may be substituted.

A-3. INTEGRATED CIRCUITS

For integrated circuits where the manufacturer is not specifically listed, any manufacturer's device of the specific type may be used.

REV. C

DRAWING 202176 C

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE NRZI. P/E & PE/NRZI FORMATTERS. MODEL NO. _____ DATE 8/20/74 SHEET 1 OF 3

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
	PRINTED WIRING BOARDS.				
1	Assy. Read Logic Pwb.	201211		3	Used on P/E.
				3	" " PE/NRZI.
2	Assy.Dead Track Detector Pwb.	201214		1	" " P/E.
				1	" " PE/NRZI.
3	Assy. Read Logic Pwb.	201217		1	" " P/E
				1	" " PE/NRZI.
4	Assy. Read Control Pwb.	201220		1	" " P/E.
				1	" " PE/NRZI.
5	Assy. Volt. Contl. OSC. Pwb.	201223-001		1	" " P/E.
				1	" " PE/NRZI.
6	Assy. Volt. Contl. OSC. Pwb.	201223-002		1	" " P/E.
				1	" " PE/NRZI.
7	Assy. State Counter Pwb.	201226		1	" " P/E.
				1	" " PE/NRZI.
8	Assy. Oscillator Pwb.	201229-000		1	" " P/E.
				1	" " PE/NRZI.
9	Assy. Oscillator Pwb.	201229-001		1	" " P/E. 10 ips.
				1	" " PE/NRZI. 10 ips.
10	Assy. Write Logic Pwb.	201232		1	" " P/E.
				1	" " PE/NRZI.
11	Assy. Write Control Pwb.	201235-000		1	" " P/E.
				1	" " PE/NRZI.
12	Assy. Write Control Pwb.	201235-001			Rewind Busy Lockout Option
13	" " " "	-002			Remote Density Select Op.
14	" " " "	-003			Rewind Busy Lockout.
					Select Unit 1. Option.
15	" " " "	-004			Rewind Busy Lockout &
					P/E Select Option.
16	Assy. Spd.Change Pwb.12½IPS.	201298		1	10 ips & 12½ ips.
17	Assy. " " " 25IPS.	201301		1	25 ips.
18	Assy. " " " 37½IPS.	201304		1	37½ ips.

CC

REV. C

DRAWING NO. 202176

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE NRZI. P/E & PE/NRZI. FORMATTERS. MODEL NO. _____ DATE 8/20/74 SHEET 2 OF [illegible]

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
19	Assy. Spd.Change Pwb.45IPS.	201307			45 ips.
20	Assy. " " " 75IPS.	201310			75 Ips.
21					
22					
23	Assy. Delay Counter Pwb.	201650-001			NRZI. .150" Head Gap.
24	Assy. " " "	-002			" .300" " "
25	Assy. CRC Generator Pwb.	201653		1	Used on NRZI.
				1	" " PE/NRZI.
26	Assy. Clock Generator Pwb.	201656		1	" " NRZI.
					" " PE/NRZI.
27	Assy.Read/Write Contl. Pwb.	201659-001			NRZI.
28	Assy. " " " "	-002			" Single Gap.
29	Assy. " " " "	-003			Rewind Busy Lockout.
					Select Unit 1. Option.
30	Assy.Write/Read Contl. Pwb.	201703-001			PE/NRZI.
31	Assy. " " " "	-002			NRZI. Select. Rewind Busy
					Lockout.
32	Assy. " " " "	-003			Remote Density Select.
33	Assy. Jumper	200289-001		1	Used on Mod 602
34	Assy. Rear Conn. Panel	201238-002		1	" " " "
35	Assy. Write Cont. Pwb.	500091-000		1	" " " 602/603
36	Assy. Read " "	500086-001		1	" " " " "
37	Assy. Read Control Pwb.	500161-001			Used on Mod 602/603
38	Assy. Write " "	500165-000			" " " " "
39	Assy. " " "	-001			" " " " "
40	Assy. " " "	-002			" " " " "
41	Assy. " " "	-003			" " " " "
42	Assy. " " "	-004			" " " " "

FORM 209 (5/74)

CC

REV. C

PART NUMBER 202176

DATE

APPROVED

WANGCO INCORPORATED

MATERIAL LIST

CODE

PART NUMBER	REV.
202176	C

TITLE NRZI. P/E & PE/NRZI FORMATTERS MODEL _____ DATE 7-17-76 SHEET 3 OF 8

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
43	Assy. Write/Read Control Pwb.	500169-000				Used on Mod 601/603
44	Assy. " " " "	-001				" " " " "
45	Assy. " " " "	-002				" " " " "
46	Assy. " " " "	-003				" " " " "
47	Assy. " " " "	-004				" " " " "

REV. C

DRAWING NO. 202176

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE NRZI. P/E & PE/NRZI FORMATTERS. MODEL NO. _____ DATE 8/20/74 SHEET 4 OF 8

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
	ELECTRONIC COMPONENTS				
1	IC, Hex Inverter 836	100084		2	Used on 201217 Assy.
				2	" " 201220 "
				2	" " 201229 "
				4	" "201235-000 "
				1	" " 201656 "
				7	" "201659-000 "
				7	" "201703-000 "
2	IC,Quad 2-Input NAND — 846	100085		6	" " 201211 "
				2	" " 201214 "
				3	" " 201220 "
				4	" " 201226 "
				4	" " 201232 "
				6	" "201235-000 "
				5	" " 201656 "
				18	" "201659-000 "
				18	" "201703-000 "
3	IC, 10-Input NAND. 1804	100087		1	" " 201217 "
				3	" "201659-000 "
				3	" "201703-000 "
4	IC, Triple 3-Input NAND 862	100107		1	" " 201214 "
				3	" " 201220 "
				1	" " 201232 "
				3	" "201235-000 "
				1	" "201650-000 "
				6	" "201659-000 "
				6	" "201703-000 "
5	IC. 844	100261		1	" " 201232 "
				1	" " 201220 "
				2	" "201659-000 "
				2	" "201703-000 "
				1	" "201235-000 "

FORM 209 (5/74)

CC

REV. C

DRAWING 2021

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE: NRZI. P/E & PE/NRZI FORMATTERS.

MODEL NO. _____ DATE 8/20/74 SHEET 5 OF 8

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
6	IC, Hex Buffer. 7407	100327		1	Used On 201235-000 Assy.
7	IC, Quad.2-Input NAND. 7400	100328		2	" " 201220 "
				3	" " 201235-000 "
8	IC, Quad 2-Input NOR. 7402	100329		6	" " 201211 "
				2	" " 201214 "
				5	" " 201220 "
				1	" " 201226 "
				1	" " 201229 "
				2	" " 201232 "
				4	" "201235-000 "
				2	" "201650-000 "
				1	" " 201653 "
				2	" " 201656 "
				9	" "201659-000 "
				9	" "201703-000 "
9	IC, Hex Inverter. 7404	100330		4	" " 201211 "
				3	" " 201220 "
				1	" " 201226 "
				2	" " 201232 "
				3	" "201235-000 "
10	IC, Hex Invert Buffer (OC)	100331		2	" " 201232 "
	7406			3	" "201659-000 "
				3	" "201703-000 "
11	IC, Quad. 2-Input AND 7408	100332		3	" " 201211 "
				1	" " 201220 "
				1	" " 201229 "
				4	" "201235-000 "
				1	" " 201656 "
				3	" "201659-000 "
				3	" "201703-000 "

FORM 209 (5/74)

CC

REV. C

DRAWING NO. 202176

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE NRZI. P/E & PE/NRZI FORMATTERS.

MODEL NO. _____ DATE 8/20/74 SHEET 6 OF 8

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
12	IC, Triple 3-Input NAND 7410	100333		1	Used on 201226 Assy.
				1	" " 201229 "
				3	" "201235-000 "
13	IC, Dual 4-Input NAND 7420	100334		1	" " 201214 "
				1	" " 201220 "
				1	" " 201226 "
14	IC, Quad. 2-Input NAND. 7437	100335		2	" " 201220 "
				1	" " 201226 "
				1	" " 201229 "
				2	" "201235-000 "
				4	" "201659-000 "
				4	" "201703-000 "
15	IC, Quad.2-Input NAND Buf.	100336		2	" " 201217 "
	7438			1	" " 201220 "
				1	" " 201229 "
				2	" " 201232 "
				8	" "201235-000 "
				3	" " 201653 "
				14	" "201659-000 "
				14	" "201703-000 "
16	IC,Dual 2-Input AND-OR Inv. 7451	100337		3	" " 201211 "
17	IC,Dual J-K MS - F/F 7473	100338		3	" " 201211 "
				6	" " 201220 "
				4	" " 201229 "
				2	" " 201232 "
				2	" "201235-000 "

CC

REV. C

DRAWING 2021/

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE: NRZI. P/E & PE/NRZI FORMATTERS. MODEL NO. _____ DATE 8/20/74 SHEET 7 OF 8

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
18	IC,Dual D-Edge Trig. F/F7474	100339		6	Used on 201211 Assy.
				1	" " 201217 "
				3	" " 201220 "
				4	" " 201226 "
				1	" " 201229 "
				1	" " 201232 "
				3	" "201235-000 "
				5	" " 201653 "
				6	" "201659-000 "
				6	" "201703-000 "
19	IC, Quad Bi-Stable Latch7475	100340		2	" " 201217 "
				2	" " 201232 "
				2	" "201235-000 "
				6	" "201659-000 "
				6	" "201703-000 "
20	IC, Quad 2-Input Exclus. - OR	100341		3	" " 201211 "
	7486			2	" " 201214 "
				2	" " 201217 "
				5	" " 201232 "
				4	" " 201653 "
				5	" "201659-000 "
				5	" "201703-000 "
21	IC,4-Bit Binary Counter.7493	100342		3	" " 201211 "
				3	" " 201220 "
				2	" " 201232 "
22	IC, 4-Bit Univ. Shift Reg.	100343		6	" " 201211 "
	7495			2	" " 201217 "
23	IC, High Speed Counter. 74197	100346		1	" " 201229 "
				2	" " 201232 "
				2	" "201650-000 "
				2	" " 201656 "

FORM 209 (5/74)

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REV. C

DRAWING NO. 202176

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202176 | REV. C

DRAWING TITLE NRZI. P/E & PE/NRZI FORMATTERS.

MODEL NO. _____ DATE 8/20/74 SHEET 8 OF 8

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
24	IC, Quad. 2-Input NOR.SP380A	100347		1	Used on 201229 Assy.
				1	" "201235-000 "
				1	" " 201656 "
				1	" "201703-000 "
25	IC,Dual 4-Input Gate W/expd	100348		2	" " 201232 "
	830			1	" "201235-000 "
				1	" "201650-000 "
				4	" " "201659-000 "
				4	" "201703-000 "
26	IC 7476	100425		1	" "201659-000 "
				1	" "201703-000 "
27	IC 7440	100426		2	" " 201653 "
28	IC 7430	100427		2	" "201659-000 "
				2	" "201703-000 "
29	IC 74107	101014		1	" " 201653 "
				4	" " 201656 "
				10	" "201659-000 "
				10	" "201703-000 "

CC

APPENDIX B

ASSEMBLY DRAWINGS

B-1 ASSEMBLY DRAWINGS

This appendix contains the assembly drawings and material lists for all assemblies and subassemblies in the Model 511 NRZI Formatter. These documents are identified in the Index, page B-3. Logic schematics and electrical information for the power supply and MTU cable are provided in Appendix C.

The assembly drawings identify every part on any given assembly or subassembly. Parts are identified either by item number (e.g., 1,2,3, etc.) or by circuit reference number (e.g., R1, C1, U1, etc.). The associated material lists incorporate these identification numbers, together with the part description, WANGCO part number, and part quantity (i.e., the quantity of a particular part required for the given assembly).

B-2 SPEED CHIP

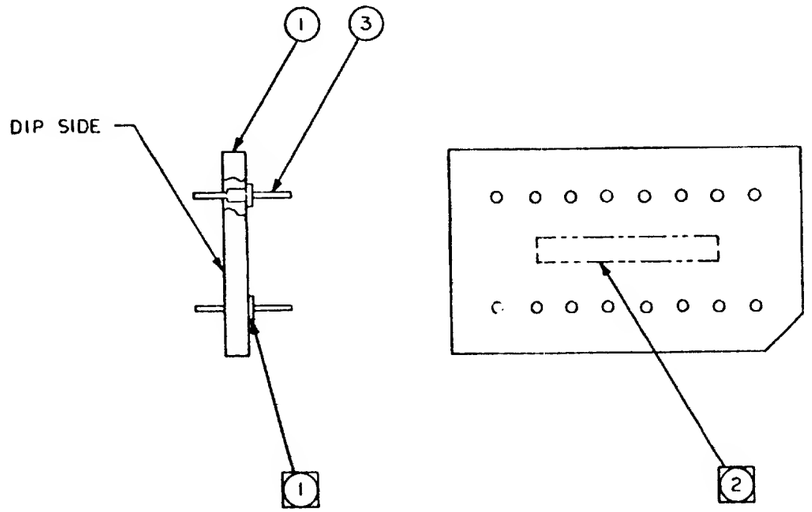
Speed Chip (speed control PWB Assembly Drawing 201301 is for the 25 ips configuration. The Speed Chip numbers applicable to other (optional) tape speeds are listed in Table B-1, and the description of other options are located in Section 4 of this manual.

TABLE B-1. Speed Chips for Standard Tape Speeds

Speed Chip P/N	Tape Speed (ips)
201298	12.5
201301	25
201304	37.5
201307	45
201310	75

APPENDIX B
MODEL 511 NRZI MAGNETIC TAPE FORMATTER
ASSEMBLY DRAWING AND MATERIAL LIST INDEX

REVISIONS				
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	ENG REL		9/14/72	
B	SEE REV. E.O. MFG REL			



[2] ASSY. NUMBER & REVISION LEVEL TO BE MARKED APPROX. WHERE SHOWN IN ACCORDANCE WITH WANGCO SPEC 100013.

[1] INSTALL PIN WITH SHOULDER MOUNTED TO UNETCHED SIDE OF BOARD.

NOTES: UNLESS OTHERWISE SPECIFIED.

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	M Miyasaki	9-15-72
2. BREAK ALL S ARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.	[illegible]	9-15-72
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY	201323	

Wang Computer Products

ASSEMBLY P.W.B.
SPEED CONTROL BD.
25 IPS

CODE	QTY. REQ'D.
F 100	1

SCALE	SIZE		
4:1	C	201301	B

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 2 OF 2

REV. E

DRAWING NO. 201301

ML

MATERIAL LIST

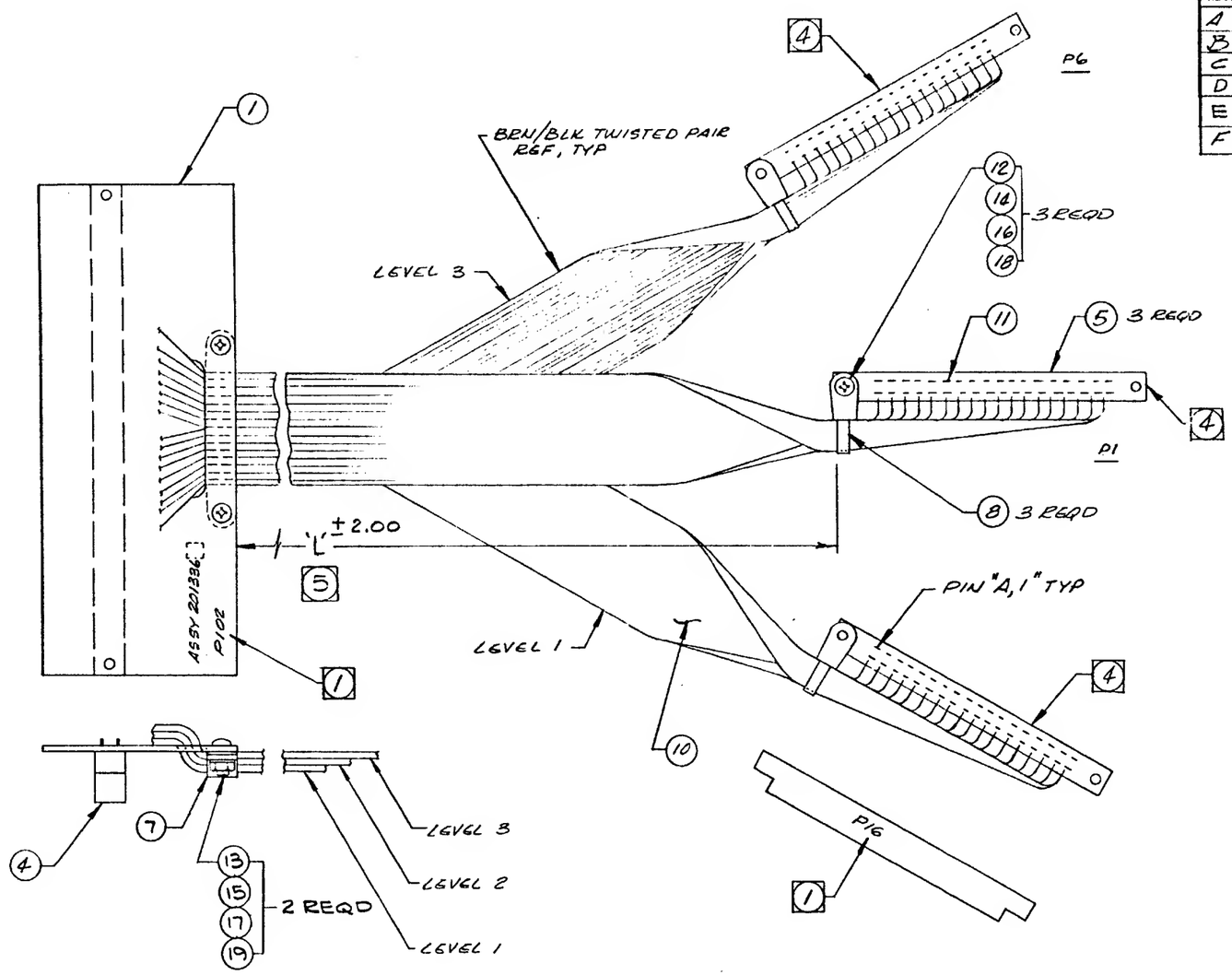
ML | DRAWING NO. 201301 | REV. B

WANGCO

DRAWING TITLE ASSEMBLY, PWB, SPEED CONTROL BD. 25 IPS MODEL NO. _____ DATE _____ SHEET 1 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed	201300	1	
2				
3	Pin	100377	16	
4				
5	Artwork, Master	201299	Ref	

REVISIONS				201335
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	ENG RELEASE	[illegible]	[illegible]	[illegible]
B	MFG. RELEASE	[illegible]	[illegible]	[illegible]
C	SEE Rev B.0		5/14/75	[illegible]
D	SEE REV E.O.		[illegible]	[illegible]
E	C210 5735	RL	8/6/75	K.S
F	CR/O 7184	[illegible]	[illegible]	[illegible]



PART NO. 201336-XXX [5] ASSY

[5] DASH NO. DENOTES LENGTH IN INCHES EG: -060 EQUALS 5FT (60 INCHES).

[4] INSTALL POLARIZATION INSERT, ITEM 9 AT P1 BETWEEN CONTACTS 5 & 6, AT P6 BETWEEN CONTACTS 3 & 4, AND AT P16 BETWEEN CONTACTS 1 & 2.

3 TERMINATE ALL UNUSED WIRES OF P1, P6, P16 & P102 IN THERMOFIT TUBING.

2. WIRE PER WIRE LIST 201337.

[1] RUBBER STAMP REF DESIGNATIONS, ASSY PART NO. & LATEST REVISION LETTER WHERE SHOWN, COLOR BLACK.

NOTES - UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	R. LIEBERMAN	8-22-72
2. BREAK ALL HARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES J	APPR	[illegible]	[illegible]
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No. FORMATTER		
	NEXT ASSY 201325		

Wang Computer Products

ASSEMBLY, MTU CABLE

CODE	QTY. REQ'D.
F 106	/

SCALE	SIZE		
FULL	C	201336 CHARTED	F
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 2 OF 2	

WANGCO INCORPORATED

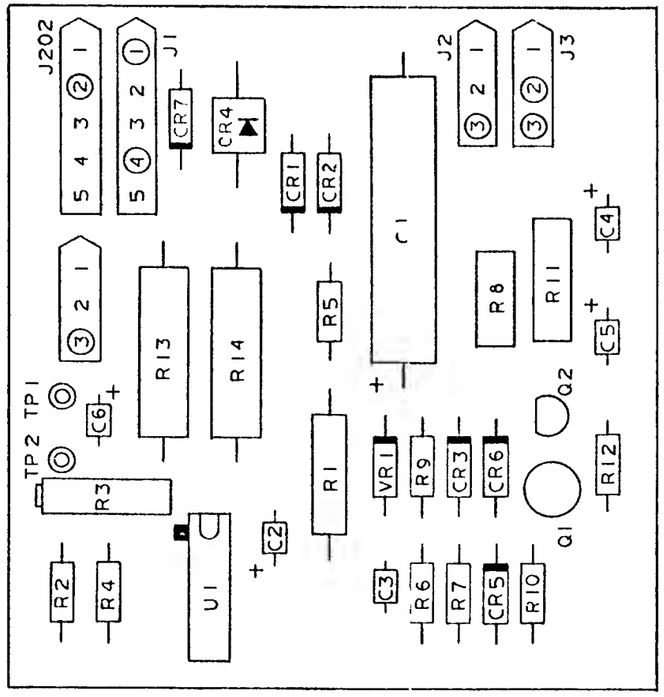
MATERIAL LIST

ML | DRAWING NO. 201336-XXX | REV. F

DRAWING TITLE ASSY. MTU CABLE. MODEL NO. Formatter. DATE 2/20/73 SHEET 1 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed.	201240-001	1	
2				
3				
4	Connector. 100 pin.	100355-001	1	P102.
5	Connector. 36 pin.	100140-001	3	P1.P6.P16.
6				
7	Clamp, Cable.	100000-007	1	
8	Strap, Cable.	100031-001	3	
9	Insert, Polarization.	100222-001	3	
10	Cable, Flat Ribbon.	100389-001	A/R	
11	Wire, Stranded Insulated.	100053-924	A/R	
12	Screw, Pan Head.	100036-210	3	4-40 x 5/8"
13	Screw, " "	100036-306	2	6-32 x 3/8"
14	Washer, Split Lock.	100042-200	3	No.4.
15	Washer, " "	100042-300	2	No.6.
16	Nut, Hex.	100043-200	3	No.4.
17	Nut, Hex.	100043-300	2	No.6.
18	Washer, Flat.	100047-200	3	No.4.
19	Washer, Flat.	100047-300	2	No.6.
20				
21				
22				
23				
24	Wire List.	201337	Ref.	

REVISIONS			201562	
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG RELEASE 4 OF 4			
B	SEE REV EO (DCR 1217)			
C	SEE REV EO (DCR 1219)			



NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L. A.	2-1-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER	
	NEXT ASSY	201581	

Wang:o Incorporated

ASSEMBLY P.W.B. POWER SUPPLY

CODE F 100

QTY. REQ'D. 1

SCALE	SIZE		
4:1	C	201562	C
DO NOT SCALE THIS DRAWING	WEIGHT		SHEET 4 OF 4

REV. C

DRAWING NO. 201562

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201562 | REV. C

DRAWING TITLE ASSY. POWER SUPPLY PWB. MODEL NO. Formatter DATE 2/6/73 SHEET 1 OF 4

ITEM NO	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS DN CKT. DESIG.
1	Board, Processed.	201561	1	
2				
3	IC. Voltage Regulator. uA723C	100108	1	U1.
4				
5	Transistor. PNP. 2N4037	100160	1	Q1.
6	Transistor. NPN. 2N4123	100080	1	Q2.
7				
8	Diode, Signal. 1N914	100091	2	CR5.CR6.
9	Diode, Rectifier. 1N4003	100127	4	CR1.CR2.CR3.CR7.
10	Diode, Rectifier. 1N4721	100052	1	CR4.
11	Diode, Zener. 6.8V. 1N4736A	100161	1	VR1.
12				
13	Capacitor, Ceramic. .005uf	100073-502	1	C3.
14	Capacitor, Tantalum. 1.5uf	100136-155	1	C4.
15	Capacitor, " 10uf	100070-106	1	C2.
16	Capacitor, " 47uf	100070-476	2	C5.C6.
17	Capacitor, Electrolytic. 200uf	100183	1	C1.
18				
19	Resistor, Variable. 1w. 1K	100163-102	1	R3.
20	Resistor. 5%. 5w. WW. .2	100111-003	2	R13.R14.
21	Resistor. " 1w. 10	100067-100	1	R11.
22	Resistor. " ¼w. 68	100156-680	1	R5.
23	Resistor. " 3w. WW. 100	100068-101	1	R1.
24	Resistor. " 1w. 120	100067-121	1	R8.
25	Resistor. " ¼w. 680	100156-681	1	R12.
26	Resistor. 1%. " 953	100155-287	1	R6.
27	Resistor. " " 1.13K	100155-294	1	R9.
28	Resistor. 5%. " 1.5K	100156-152	1	R2.
29	Resistor. " " 4.3K	100156-432	1	R4.
30	Resistor. 1%. " 4.32K	100155-350	1	R7.
31	Resistor. " " 5.11K	100155-357	1	R10.
32		B-15		

REV. C

DRAWING N 201562

ML

WANGCO

MATERIAL LIST

ML | DRAWING NO. 201562 | REV. C

DRAWING TITLE ASSY. POWER SUPPLY PWB. MODEL NO. Formatter DATE 2/6/73 SHEET 2 OF 4

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
33	Connector, 5 pin.	100247-005	1	J202.
34	Connector, 5 pin.	100247-008	1	J1.
35	Connector, 3 pin.	100247-010	2	J2.J4.
36	Connector, 3 pin.	100247-011	1	J3.
37				
38				
39	Test Point Pin.	100098	2	TP1.TP2.
40	Pad, Transistor. TO-5.	100223	1	Use with item 5.
41				
42				
43	Artwork, Master.	201560	Ref.	

REVISIONS				201581
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG RELEASE			
B	SEE REV. E.O.			
C	SEE REV. E.O.			
D	SEE CH/O 3029			
E	SEE CR/O 3418			
F	C/O 3593			

DETAIL F

DETAIL E
2 PLACES

REF-MICA WASHER SUPPLIED WITH DIODE

SEE DETAIL E

SEE DETAIL F

VIEW D-D

VIEW A-A

SECTION B-B

SECTION C-C

2 REQD 33 31 34 P2

33 31 34 P4

2 REQD 34 32 2 REQD 33 P1

33 31 34 P3

23 2 REQD

26

67 85 2 REQD

11

2 REQD 35 36

1.5A SB F201

10A F202

TB201

37

2 REQD 5

69 85 2 REQD

90 4 REQD

68 81 3 REQD

68 81 78 2 REQD

9 REF

41

15

65 84 4 REQD

73 86 2 REQD

17

39 3 REQD

1 REF

13

6 REF

1

9

40 26 REQD

28

66 84 4 REQD

29 2 REQD

67 85

3

J2 J3 J4

REF 23

60

A

53 12 REQD

25

45 71 85

52

49

72 82 6 REQD

72 4 REQD

92 4 REQD

21

20

10

66 80 89 2 REQD

B

C

D

56 57 58

68 81 2 REQD

59 60

68 81 90 4 REQD

22

7

8

AIR FLOW

5 2 REQD

24

6

67 85 2 REQD

27 29

69 2 REQD 81 90 4 REQD

14

6 REF

69

20 REF

61

50

75

10 REF

90

9 REF

REF 40

40 REF

90

85

70

68

21 REF

61

51

10 REF

90

85

75 2 REQD

9 REF

81

42

90

84

40 REF

91

2. WIRE PER WIRE LIST 201759.

1. IDENTIFY PER WANGCO SPEC 100037,TA

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR XXX± ±	DRAWN		
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No. FORMATTER	SCALE 1:1	SIZE D
	NEXT ASSY 201514 201323 201515	DO NOT SCALE THIS DRAWING	WEIGHT

Wangco Incorporated

ASSEMBLY, POWER SUPPLY

201581 CANCELLED

F

SHEET 4 OF 5

B-17

REV. -

DRAWING NO. 201581-001

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201581-001 | REV. F

DRAWING TITLE ASSY. POWER SUPPLY. MODEL NO. Formatter DATE 5/18/73 SHEET 1 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Assy. Regulator Pwb.	201562	1	
2				
3	Spec; Proc. Power Transformer	200264	1	T1.
4				
5	Stand-Off. Term. Board Cover	201256	4	
6	Support, Left Hand.	201289	1	
7	Bracket, Fan Mounting.	201295-001	1	
8	Bracket, " "	-002	1	
9	Chassis, Power Supply.	201557	1	
10	Heatsink.	201558	1	
11	Panel, Power Supply.	201616	1	
12	Bracket, Component Mtg.	201778	1	
13	Clamp, Capacitor.	201784	1	
14	Decal, Voltage.	201785	1	
15	Insulator.	201788	1	
16				
17	Capacitor, Elect. 65,000uf	100029-007	1	C2.
18	Diode, Power. 1N3208	100174	2	CR1. CR2.
19	Rectifier, SC. 2N3668	100413	1	SCR1.
20	Transistor, PNP. TI.P30	100113	1	Q1.
21	Transistor, NPN. 2N3771	100173	1	Q2.
22	Fan. 50/60Hz.	100388	1	M101.
23	Strip, Marker.	100024-003	2	Use with item 26.
24	Strip, "	100048-006	2	Use with item 27.
25	Strip, "	100421-008	1	Use with item 28.
26	Block, Terminal.	100044-003	1	TB201.
27	Block, "	100023-006	1	TB202.
28	Block, "	101119-008	1	TB1.
29	Jumper, 2 Terminal.	100150	2	Use with item 28.
30				
31	Connector.	100010-003	3	P2.P3.P4.
32	Connector.	-005	1	P1.

REV. F

DRAWING NO. 201581-001

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201581-001 | REV. F

DRAWING TITLE ASSY. POWER SUPPLY. MODEL NO. Formatter DATE 5/18/73 SHEET 2 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
33	Pin, Female.	100021-004	6	
34	Pin, Male.	-010	5	
35	Fuseholder.	100027	2	
36	Fuse. "Slo-Blo" 1.5 amp	100235-015	1	F201.
37	Fuse. 10 amp	100028-027	1	F202.
38	Terminal, Ins. Ring Tongue.	100055-002	1	
39	Terminal, " " "	-004	3	
40	Terminal, " " "	100057-004	26	
41	Terminal, " " "	-008	1	
42	Lug, Solder.	100138-002	1	
43	Lug, "	-005	2	
44				
45	Spacer, Round.	100093-008	1	
46				
47	Grommet, Clamp.	100227-006	1	
48	Grommet, "	-010	1	
49	Grommet, Caterpillar.	100141-001	A/R	
50	Insulator, Transistor	100146	1	Use with item 20.
51	Insulator, "	100151	2	Use with items 19 & 21.
52	Strap, Cable.	100031-003	1	
53	Strap, "	100171-001	12	
54				
55	Wire, Solid Bare.	100051-016	A/R	
56	Wire, Insulated.	100053-912	A/R	
57	Wire, "	-914	A/R	
58	Wire, "	-918	A/R	
59	Wire, Twisted Pair.	100054-018	A/R	
60	Tubing, Shrink.	100185-005	A/R	
61	Tubing, Teflon.	100226-018	A/R	
62				
63				
64				

REV. F

DRAWING NO. 201581 - C01

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201581 - 001 | REV. F

DRAWING TITLE ASSY. POWER SUPPLY. MODEL NO. Formatter DATE 5/18/73 SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
65	Screw, Pan Head.	100036-204	4	4-40 x 1/4"
66	Screw, " "	-208	6	4-40 x $\frac{1}{2}$"
67	Screw, " "	-304	5	6-32 x $\frac{1}{4}$"
68	Screw, " "	-306	15	6-32 x 3/8"
69	Screw, " "	-310	6	6-32 x 5/8"
70	Screw, " "	-312	1	6-32 x 3/4"
71	Screw, " "	-320	1	6-32 x 1.25"
72	Screw, " "	-406	10	8-32 x 3/8"
73	Screw, " "	-506	2	10-32 x 3/8"
74				
75	Washer, Nylon Shoulder.	100063-001	5	
76	Washer, " "	-005	2	
77				
78	Washer, Flat.	100047-300	2	No.6.
79				
80	Washer, Split Lock.	100042-200	2	No.4.
81	Washer, " "	-300	19	No.6.
82	Washer, " "	-400	6	No.8.
83				
84	Washer. Int. Tooth Lock.	100059-200	8	No.4.
85	Washer, " " "	-300	14	No.6.
86	Washer, " " "	-500	2	No.10.
87	Washer, " " "	-600	2	$\frac{1}{4}$.
88				
89	Nut, Hex.	100043-200	2	4-40.
90	Nut, "	-300	20	6-32.
91	Nut, "	-510	2	$\frac{1}{4}$-28.
92				
93	Nut, Speed.	101200-003	4	
94				
95	Wire List.	201759	Ref.	
96	Test Procedure.	201760	Ref.	

F 100

100 volt.

WANGCO INCORPORATED

MATERIAL LIST

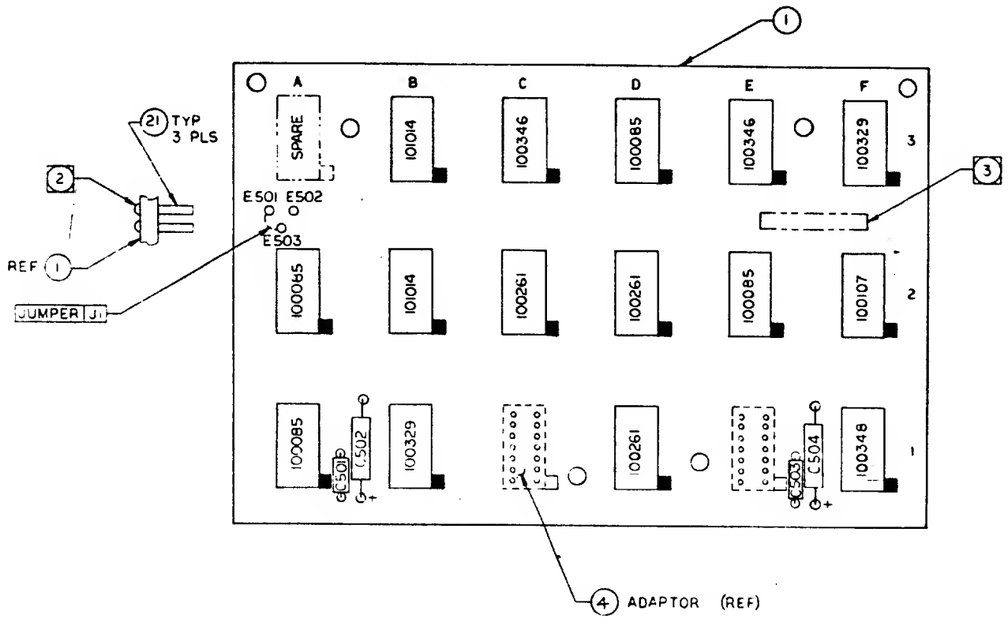
ML | DRAWING NO. 201581 - 002 | REV. F

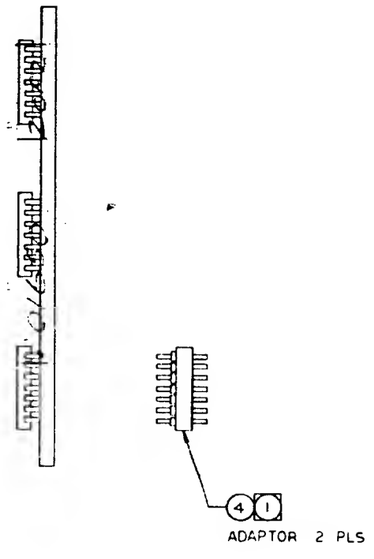
DRAWING TITLE ASSY. POWER SUPPLY. MODEL NO. Formatter DATE 5/18/73 SHEET 1 OF 1

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
	USE MATERIAL LIST 201581-001			
	EXCEPT:-			
3	Spec;Proc. Power Transformer.	200264	1	Delete.
3	Spec;Proc. Power Transformer.	201066	1	Add.
14	Decal, Voltage.	201785	1	Delete.
14	Decal, Voltage.	201080-002	1	Add.

REVISIONS				
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG. REL.			
B	SEE CH/O 3448		4/14/	

ASSY, PWB DELAY COUNTER NRZ





3 RUBBER STAMP REV LEVEL PER WANG SPEC 100013

2 TRIM WIRE WRAP PINS FLUSH WITH BOARD ON DIP SIDE.

1 INSTALL ADAPTOR WITH LARGE PIN MOUNTED TO DIP SIDE OF P.C.BOARD AS SHOWN.

NOTES UNLESS OTHERWISE SPECIFIED

PART NO 201650-XXX SEE TABULATED M/L

NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR, XXX± ±	DRAWN		
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No. FORMATTER		
	NEXT ASSY		

Wangco Incorporated

ASSEMBLY, PWB DELAY COUNTER NRZ

CODE F12?

QTY. REQ'D 1

SCALE 2:1 | SIZE D | 201650 CHARTED | B

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 2 OF 2

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201650-000 | REV. B

ASSY. PWB

DRAWING TITLE DELAY COUNTER - NRZ MODEL NO. Formatter DATE 4/4/74 SHEET 1 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed	201649	1	
2				
3				
4	Board, Comp. Mounting.	100353-014	2	C1,E1.
5				
6				
7	IC. 15846	100085	4	A1,A2,E2,D3.
8	IC. 15862	100107	1	F2.
9	IC. 7402	100329	2	B1,F3.
10	IC. 8291	100346	2	C3,E3.
11	IC. 830	100348	1	F1.
12	IC. 844	100261	3	D1,C2,D2.
13	IC. 74107	101014	2	B2,B3.
14				
15				
16	Capacitor, Ceramic 1uf	100364-104	2	C501,C503.
17	Capacitor, Tantl. 35V 4.7uf	100363-475	2	C502,C504.
18				
19				
20				
21	Pin, Wire-Wrap.	100360	3	E501,502,503.
22				
23				
24				
25				
26	Printed Master.	201648	Ref.	
27	Test Procedure, Module	200636	Ref.	
		B-25		

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201650-001 | REV. -

DRAWING TITLE: ASSY. PWB DELAY COUNTER - NRZI.150 R to W HEAD GAP

MODEL NO. Formatter DATE 4/4/74 SHEET 1 OF ____

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
	USE MATERIAL LIST 201650-000			
	EXCEPT:-			
22	Wire, Solid, Insulated	100383-930	A/R	Add Jumper J1 from E501 to E503.

WANGCO INCORPORATED

MATERIAL LIST

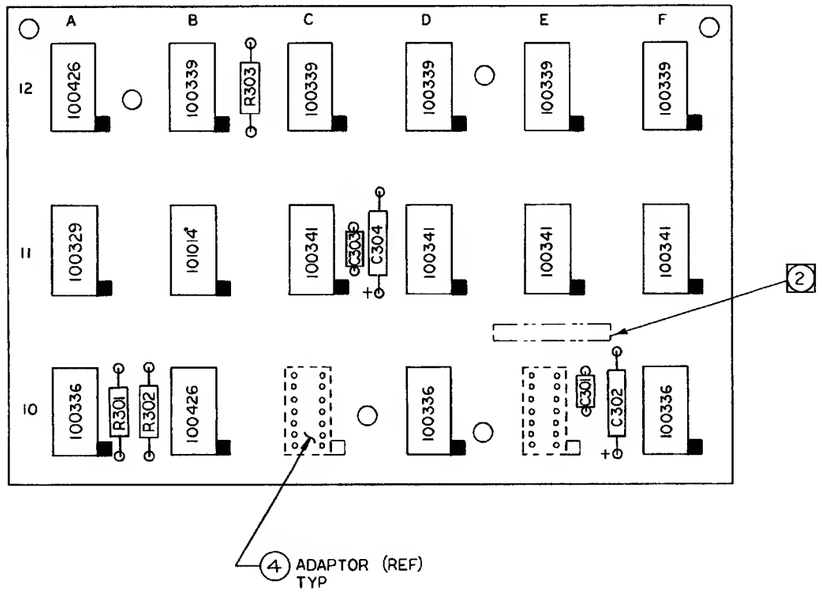
ML | DRAWING NO. 201650-002 | REV. F

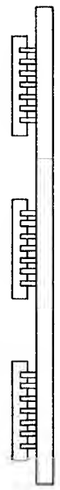
DRAWING TITLE: ASSY. PWB DELAY COUNTER - NRZI.300 R to W HEAD GAP

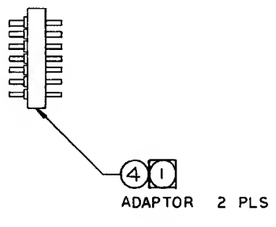
MODEL NO. Formatter DATE 4/4/74 SHEET 1 OF 1

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
	USE MATERIAL LIST 201650-000			
	EXCEPT:-			
22	Wire, Solid, Insulated	100383-930	A/R	Add Jumper J1 from E502 to E503.

REVISIONS				201653 A
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG. REL.		6/14/73	







2 RUBBER STAMP REV LEVEL PER WANG SPEC 100013.

1 INSTALL ADAPTOR WITH LARGE PIN MOUNTED TO DIP SIDE OF P.C. BOARD AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	M. Miyasato	6-21-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES ✓	APPR.		6/14/73
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER	
	NEXT ASSY	200685 200686	

Wangco Incorporated

ASSEMBLY, PWB
CRC GENERATOR
NRZ

CODE F100 | DWG. REQ'D. 1

SCALE 2:1 | SIZE D | 201653 | A

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 2 OF 2

WANGCO INCORPORATED

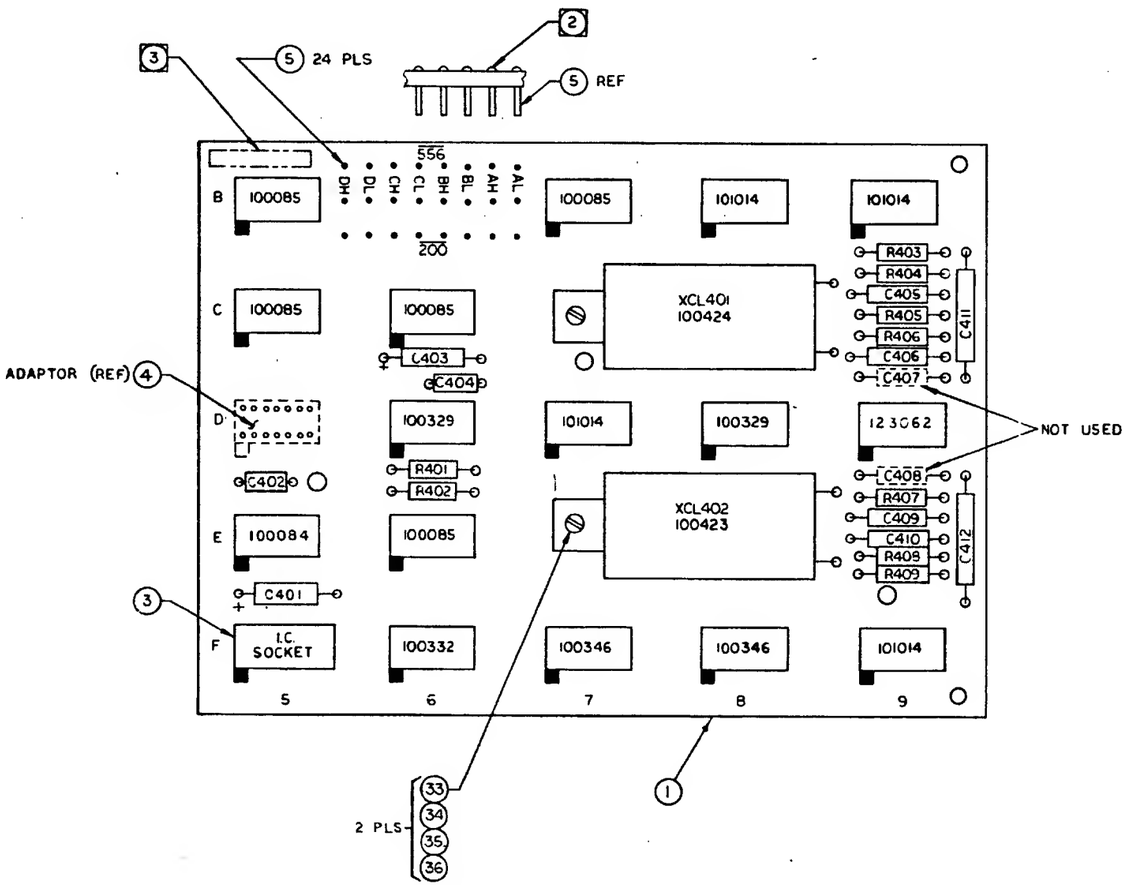
MATERIAL LIST

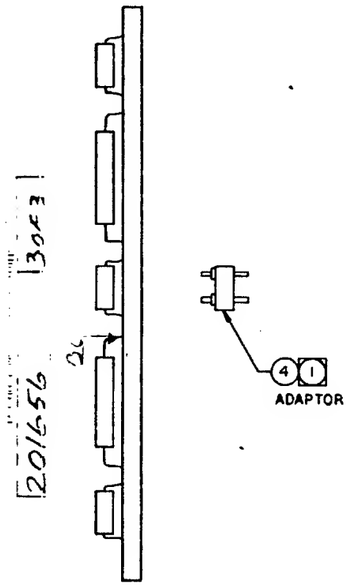
ML | DRAWING NO. 201653-001 | REV. A

DRAWING TITLE: ASSEMBLY, PWB CRC GENERATOR - NRZ | MODEL NO: FORMATTER | DATE | SHEET 1 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed	201652-001	1	
2				
3				
4	Board, Comp. Mounting	100353-014	2	C10, E10
5				
6				
7	IC 7402	100329-001	1	A11
8	IC 7438	100336-001	3	A10, D10, F10
9	IC 7474	100339-001	5	B12,C12,D12,E12,F12
10	IC 7486	100341-001	4	C11,D11,E11,F11
11	IC 7440	100426-001	2	B10,A12
12	IC 74107	101014-001	1	B11
13				
14				
15				
16	Capacitor, Ceramic 1µf	100364-104	2	C301, C303
17	Capacitor, Tantl 35V4.7µf	100363-475	2	C302, C304
18				
19				
20				
21	Resistor, ¼w 5% 220	100156-221	1	R302
22	Resistor, ¼w 5% 560	100156-561	1	R303
23	Resistor, ¼w 5% 3.3K	100156-332	1	R301
24				
25				
26				
27	Printed Master	201651-001	0	
28				
29	Test Procedure, Module	200630-001	0	

REVISIONS				201656
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG. REL.			
B	SEE CR/O 3320			
C	CR/O 6364			





3 RUBBER STAMP REV LEVEL PER WANG SPEC 100013.

2 TRIM WIRE WRAP PINS FLUSH WITH BOARD ON DIP SIDE.

1 INSTALL ADAPTOR WITH LARGE PIN MOUNTED TO DIP SIDE OF P.C. BOARD AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN		
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES	MATERIAL		
	FINISH		
	MODEL No. 501, 502, 503, 504, 505, 506, 508	SCALE 2:1	SIZE D
	NEXT ASSY 200[illegible]	DO NOT SCALE THIS DRAWING	WEIGHT

Wangco Incorporated

ASSEMBLY, P W B
CLOCK GENERATOR
NRZ

COL	F
12	
QTY REQ.	1

201656 C

SHEET 3 OF 3

B-33 1

CODE F120

REV. U | PART NUMBER 201656-001 | DATE | APPROVED

WANGCO INCORPORATED

MATERIAL LIST

PART NUMBER	REV.
201656-001	C

TITLE ASSEMBLY, PWB CLOCK GENERATOR - NRZ

MODEL 501,504,511,601, 503,513,603 DATE 2-3-76 SHEET 1 OF 3

ITEM NO.	DESCRIPTION	PART NO.	REQD	REV.		REMARKS
						NEXT ASSEMBLY/USED ON
						200685,200686 500106,500107
1	Board. Processed	201655-001	1			
2						
3	Socket, IC 16 pins	100352-001	1			F5.
4	Board, Comp Mounting	100353-014	1			D5.
5	Pin, W/W	100360-001	24			
6						
7						
8	Crystal 125.1 KHz	100423-001	1			XCL 402.
9	Crystal 180 KHz	100424-001	1			XCL 401.
10						
11						
12	IC 15836	100084-001	1			E5.
13	IC 15846	100085-001	5			B5,C5,C6,E6,B7.
14	IC 7402	100329-001	2			D6,D8.
15	IC 7408	100332-001	1			F6.
16	IC 8291	100346-001	2			F7,F8.
17	IC SP380	123062-001	1			D9.
18	IC 74107	101014-001	4			D7,B8,B9,F9.
19						
20						
21	Capacitor, Mylar .047uf	100366-473	4			C405,406,409,410.
22	Capacitor, Mylar .0022uf	100165-222	1			C411.
23	Capacitor, Mylar .0033uf	100165-332	1			C412.
24	Capacitor, Ceramic 1uf	100364-104	2			C402,404.
25	Capacitor, 35V 4.7uf	100363-475	2			C401,403.
26						
27						
28	Resistor, 5%, ¼W 3.3K	100156-332	2			R401, 402.
29	Resistor, " " 560	100156-561	1			R403.
30	Resistor, " " 1K	100156-102	2			R404,409.
31	Resistor, " " 10K	100156-103	4			R405,406,407,408.
32						

REV. C

PART NUMBER 201656-001

DATE

APPROVED

WANGCO INCORPORATED

MATERIAL LIST

CODE
F120

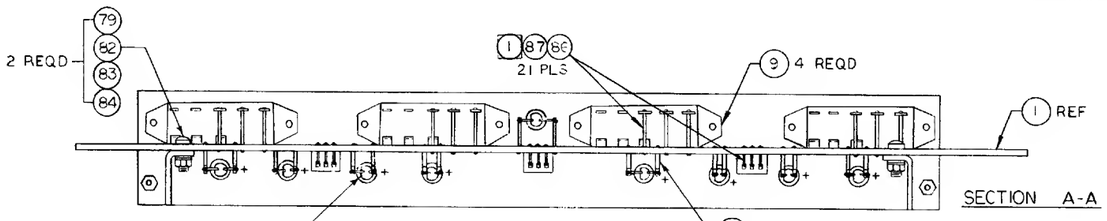
PART NUMBER	REV.
201656-001	C

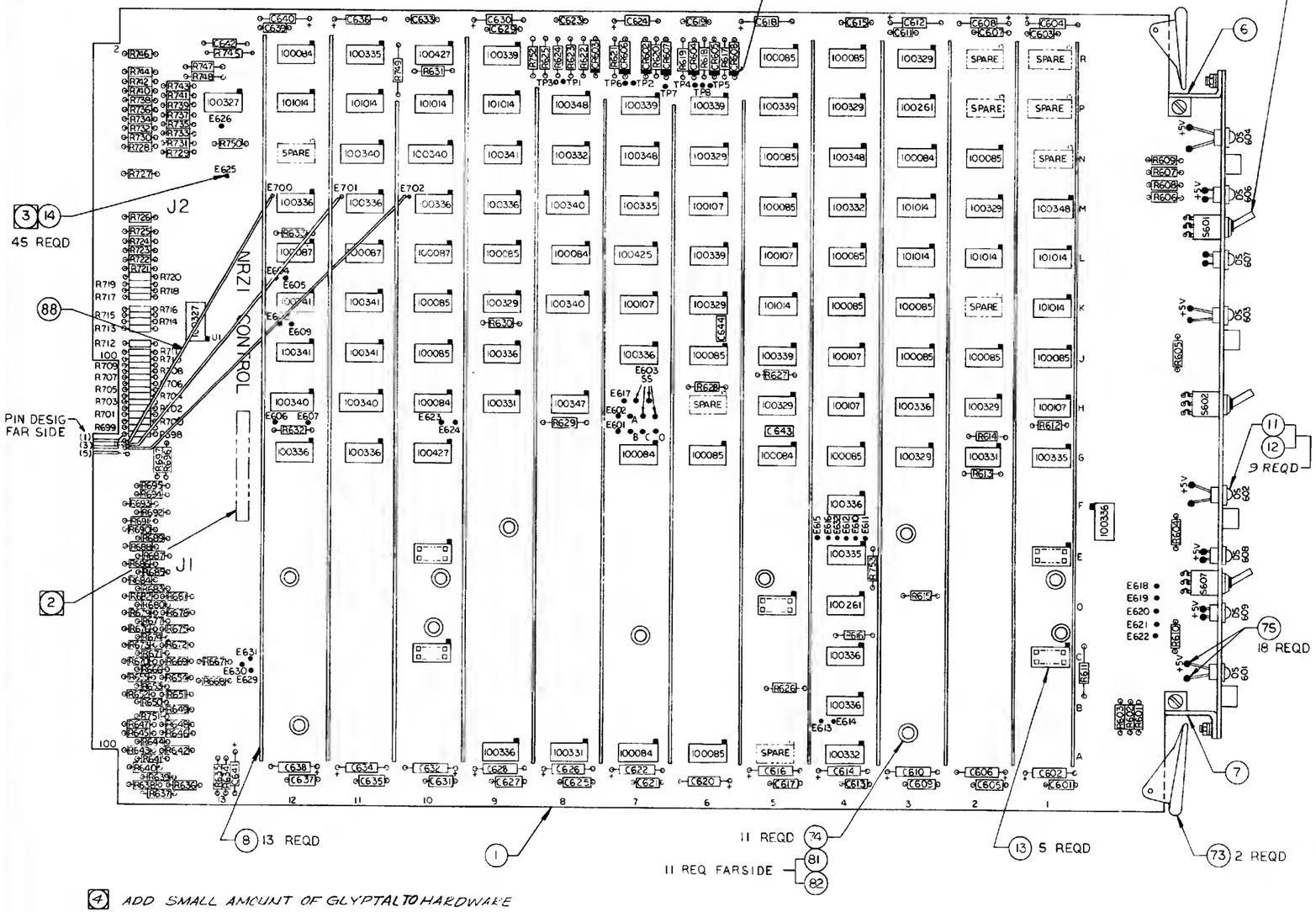
TITLE ASSEMBLY, PWB CLOCK GENERATOR - NRZ

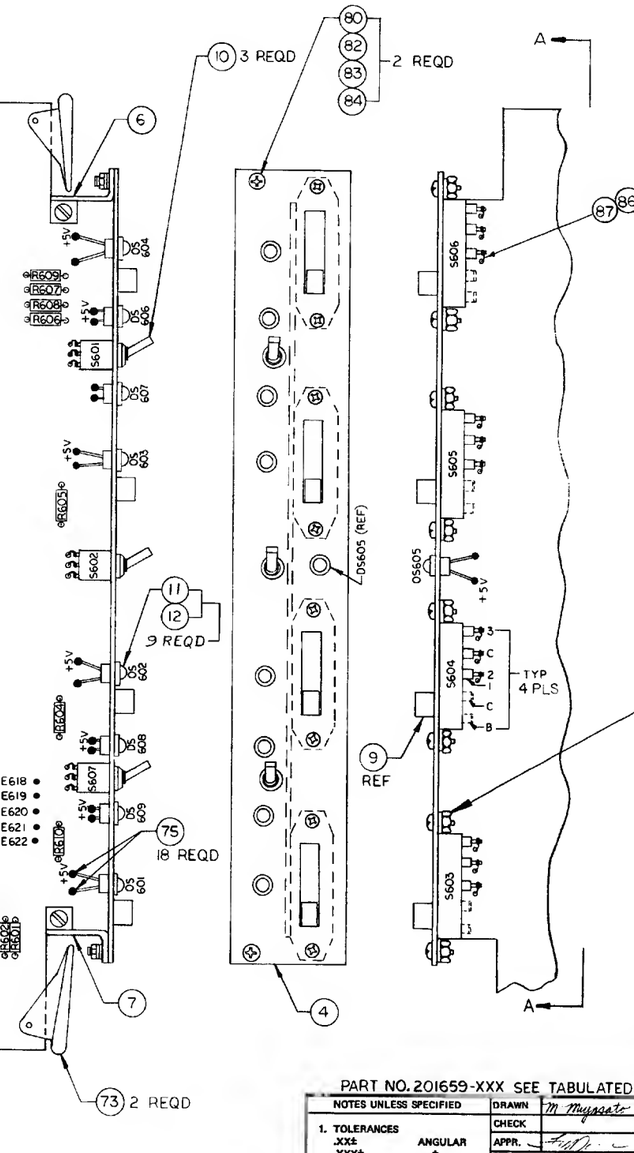
MODEL 501,504,511,601, 503,513,603 DATE 2-3-76 SHEET 2 OF 3

ITEM NO.	DESCRIPTION	PART NO.	REQD	REV.		REMARKS
						NEXT ASSEMBLY/USED ON
33	Screw, Pan Head	100036-104	2			2-56 x ¼"
34	Washer, Split Lock	100042-100	2			No. 2
35	Washer, Flat	100047-100	2			No. 2
36	Nut, Hex.	100043-100	2			2-56
37						
38						
39						
40						
41	Printed Master	201654-001	0			
42						
43	Test Procedure, Module	200636-001	0			
44						

REVISIONS				201659
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG REL			
B	SEE CR/O 3002			
C	SEE CR/O 3068			
D	SEE CR/O 3449			
E	SEE CR/O 4360			
F	CR/O 5863			
G	SEE CR/O 6375			
H	CR/O 8272			







4 ADD SMALL AMOUNT OF GLYPTAL TO HARDWARE

3 JUMPER PINS; JUMPER LOCATIONS PER DASH VERSIONS SEE NEXT ASSEMBLY.

2 RUBBER STAMP ASSY NO AND LATEST REV LETTER PER WANGCO SPEC 100013.

1 WIRE TERMINALS B,C,2,1,C,3 OF S3,S4,S5, S6 TO CORRESPOND TO TERMINALS ON CONTROL BOARD

NOTES: UNLESS OTHERWISE SPECIFIED

PART NO. 201659-XXX SEE TABULATED M/L ASSY

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	M Mysaate	7/5/73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER	
	NEXT ASSY	20068S	

Wangco Incorporated

ASSEMBLY, PWB
WRITE/READ CONTROL
NRZI

CODE F120 | QTY. REQ'D. 1

SCALE	SIZE	
FULL	D	201659 (CHARTED) H

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 5 OF 5

B-37

REV. H

DRAWING NO. 201659-000

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201659-000 | REV. 1

DRAWING TITLE: ASSY. PWB WRITE/READ CONTROL, NRZI

MODEL NO: Formatter DATE: 4/4/74 SHEET 1 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed	201658-001	1	MIN REV 'E'
2				
3				
4	Panel, Front	201701-001	1	Min Rev 'C'
5				
6	Brackets, Support	201246-001	1	
7	Brackets, "	-002	1	
8	Bar, Buss.	201249-001	13	
9	Switch, Slide, Modified	201321-001	4	S603,604,605,606.
10	Switch, Toggle	101102-001	3	S601,602,607.
11	Diode, Light Emitting	100385-001	9	DS601,602,603,604,605,606,
				DS607,608;609.
12	Clip, Mounting	100386-002	9	Use with item 11
13	Socket, Solder Tail,IC.	100351-001	5	C1,E1,D5,C10,E10.
14	Pin, W/W	100360-001	45	
15				
16				
17				
18	IC. 836	100084-001	7	N3,G5,A7,G7,L8,H10,R12.
19	IC. 846	100085-001	18	J1,J2,N2,J3,K3,G4,K4,L4,
				R4,M5,N5,A6,G6,J6,L9,J10,
				K10,R5.
20	IC. 1804	100087-001	3	L10,L11,L12.
21	IC. 862	100107-001	6	H1,H4,L5,M6,K7,J4.
22	IC. 844	100261-001	2	P3,D4.
23	IC. 7407	100327-001	2	U1,P13.
24	IC. 7402	100329-001	9	H2,M2,G3,R3,P4,H5,K6,N6,
				K9.
25	IC. 7406	100331-001	3	G2,A8,H9.
26	IC. 7408	100332-001	3	A4,M4,N8,
27	IC. 7437	100335-001	4	G1,E4,M7,R11.

REV. H
DRAWING NO. 201659-000
ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201659-000 | REV. H

DRAWING TITLE: ASSY. PWB WRITE/READ CONTROL, NRZI
MODEL NO. Formatter
DATE 4/4/74
SHEET 2 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
28	IC. 7438	100336-001	14	F1,H3,J4,C4,F4,J7,A9,J9,M9,
				M10,G11,M11,G12,M12.
29	IC. 7474	100339-001	6	J5,P5,L6,P6,P7,R9.
30	IC. 7475	100340-001	6	K8,M8,N10,H11,N11,H12.
31	IC. 7486	100341-001	5	N9,J11,K11,J12,K12.
32	IC. 8T380	100347-001	1	H8.
33	IC. 830	100348-001	4	M1,N4,N7,P8.
34	IC. 7430	100427-001	2	G10,R10.
35	IC. 7476	100425-001	1	L7.
36	IC. 74107	101014-001	10	K1,L1,L2,L3,M3,K5,P9,P10,
				P11,P12.
37				
38				
39				
40				
41	Diode IN277	100361-001	7	CR602,603,604,605,606,607,
				CR608.
42				
43				
44				
45				
46	Capacitor, Sil.Mica 150pf	100243-151	1	C642.
47	Capacitor, Ceramic 1uf	100364-104	19	C601,603,605,607,609,611,
				C613,615,617,619,621,623,625,
				C627,629,631,633,635,637,639.
48	Capacitor, Tant. 35V 4.7uf	100363-475	20	C602,604,606,608,610,612,
				C614,616,618,620,622,624,
				C626,628,630,632,634,636,
				C638,640.
49	Capacitor 39uf	100363-396	1	C641.
50	Capacitor 330pf	100243-331	2	C643,644.
51				

REV. H

DRAWING NO. 201659-000

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201659-000 | REV. H

DRAWING TITLE ASSY. PWB WRITE/READ CONTROL, NRZI

MODEL NO. Formatter DATE 4/4/74 SHEET 3 OF 5

ITEM NO.	DRAWING TITLE		DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
52					
53					
54	Resistor, 1%.⅛W.	150	100155-210	1	R622.
55	Resistor, " "	301	-239	1	R619.
56	Resistor, " "	590	-267	1	R618.
57	Resistor, " "	909	-285	1	R621.
58	Resistor, " "	1K	-289	1	R624.
59	Resistor, " "	1.5K	-306	1	R620.
60	Resistor, " "	2.32K	-324	1	R617.
61					
62					
63	Resistor, 5%.¼W.	220	101156-221	65	R601,602,603,604,605,606,
					R608,609,614,637,638,641,
					R642,645,650,652,653,654,
					R666,672,673,674,675,677,
					R678,679,680,681,682,683,
					R684,685,686,687,688,689,
					R691,696,711,712,713,714,
					R715,716,717,718,719,720,
					R721,722,723,724,725,726,
					R727,728,730,732,734,736,
					R738,740,742,744,746,
64	Resistor, 5%.¼W.	330	101156-331	14	R625,667,668,729,731,733,
					R735,737,739,741,743,745,
					R749,750.
65	Resistor, 5%.¼W.	560	101156-561	5	R611,612,623,627,752.
66	Resistor, " "	1K	-102	41	R616,628,632,636,639,640,
					R643,644,646,647,648,649,651,
					R655,669,670,671,676,690,692,
					R693,694,695,697,698,699,700,
					R701,702,703,704,705,706,707,
					R708,709,710,747,748,751,753.

REV. H

DRAWING NO. 201659-000

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 201659-000 | REV. H

DRAWING TITLE ASSY. PWB WRITE/READ CONTROL, NRZI

MODEL NO. Formatter DATE 4/4/74 SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
67	Resistor, 5%.¼W. 3.3K	101156-332	9	R607,610,613,615,626,629,
				R630,631,633.
68	Resistor, 5%.¼W. 10K	101156-103	1	R634.
69	Resistor, " " 20K	-203	1	R635.
70				
71				
72				
73	Extractor, Card/Roll Pin	100354-001	2	
74	Spacers, Round Thd.	100060-015	11	4-40 X 7/16"
75	Terminal, Swaged	100376-001	18	
76				
77				
78	Screw, Flat Head.	100040-103	8	2-56 x 3/16
79	Screw, Pan Head	100036-206	2	4-40 X 3/8"
80	Screw, Flat Head	100040-205	2	4-40 X 5/16"
81	Screw, Pan Head	100036-204	11	4-40 X 1/4"
82	Washer, Split Lock	100042-200	15	
83	Washer, Flat	100047-200	4	
84	Nut, Hex.	100043-200	4	
85	Nut, "	" -100	8	No. 2-56
86	Wire, Solid, Bare	100051-024	A/R	
87	Tubing, Teflon	100226-024	A/R	Use with item 86.
88	Wire 26 Ga Insulated.	100248-926	A/R	Jumper E700 to J1-1
				E701 to J1.1.
				E702 to J1-3
	Printed Master	201657-001	0	
	Test Procedure	200636-001	0	
	Schematic	200452-001	0	

REV. G

PART NUMBER 201659-001

APPROVED RK DATE 9-10-75

WANGCO INCORPORATED

MATERIAL LIST

CODE F120

PART NUMBER	REV.
201659-001	G

TITLE ASSY. PWB. WRITE/READ CONTROL, NRZI. MODEL Formatter. DATE 9/9/75 SHEET 1 OF 1

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD/DELETE THE FOLLOWING:-	201659-000		H		NEXT ASSEMBLY/USED ON
95	Wire, Solid Insulated.	100383-930	A/R			Add Jumpers:
						E613 to E614
						E619 to E620
						E621 to E622
						E625 to E626
						E629 to E630

FORM 209 (R.12/74)

REV. G

PART NUMBER 201659-002

DATE 9-10-75

APPROVED TD

CODE F120

WANGCO INCORPORATED

MATERIAL LIST

PART NUMBER	REV.
201659-002	G

TITLE ASSY. PWB. NRZI WRITE/READ CONTROL - SINGLE STOCKS (ALL UNITS) MODEL Formatter. DATE 9/9/75 SHEET 1 OF 1

ITEM NO.	DESCRIPTION	PART NO.	REQD	~~MIN.~~ REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD/DELETE THE FOLLOWING:-	201659-000		H		NEXT ASSEMBLY/USED ON
95	Wire, Solid Insulated.	100383-930	A/R			Add Jumpers:
						E613 to E614
						E619 to E620
						E621 to E622
						E629 to E630
						E603 to A,B,C,D

FORM 209 (R.12/74)

REV. G

PART NUMBER 201659-003

DATE 9-10-75

APPROVED [illegible]

WANGCO INCORPORATED

MATERIAL LIST

CODE	
F120	
PART NUMBER	REV.
201659-003	G

TITLE ASSY. PWB. NRZI WRITE/READ CONTROL REWIND BUSY LOCKOUT. SELECT FAD 1 MODEL Formatter. DATE 9/9/75 SHEET 1 OF 1

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD/DELETE THE FOLLOWING:-	201659-000		H		NEXT ASSEMBLY/USED ON
95	Wire, Solid Insulated.	100383-930	A/R			Add Jumpers:
						E601 to E602
						E610 to E612
						E613 to E614
						E619 to E620
						E621 to E622
						E625 to E626
						E629 to E630.

FORM 209 (R.12/74)

HARRIS CORP.
COMPUTER SYSTEMS DIV.

INHIBIT 0 →12, 12 →0 CONVERSION FOR 7CH. EVEN PARITY

CODE
F120

WANGCO INCORPORATED

MATERIAL LIST

PART NUMBER	REV.
201659-004	C

TITLE ASSY. PWB NRZI WRITE/READ CONTROL REWIND BUSY LOCKOUT. MODEL 511 DATE 9/9/75 SHEET 1 OF 1

REV. C

PART NUMBER 201659-001

APPROVED DATE 9-10-75

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD/DELETE THE FOLLOWING:-	201659-000		H		NEXT ASSEMBLY/USED ON
95	Wire, Solid Insulated.	100383-930	A/R			Add Jumpers:
						E601 to E602
						E604 to E605
						E613 to E614
						E619 to E620
						E621 to E622
						E623 to E624
						E625 to E626
						E629 to E630

FORM 209 (R.12/74)

WANGCO NOVA TAPE CONTROLLER SYSTEMS.

CODE F120

WANGCO INCORPORATED

MATERIAL LIST

PART NUMBER	REV.
201659-005	C

TITLE ASSY. PWB. NRZI WRITE/READ CONTROL. MODEL 501 DATE 6/28/75 SHEET 1 OF 1

REV. C

PART NUMBER 201659-005

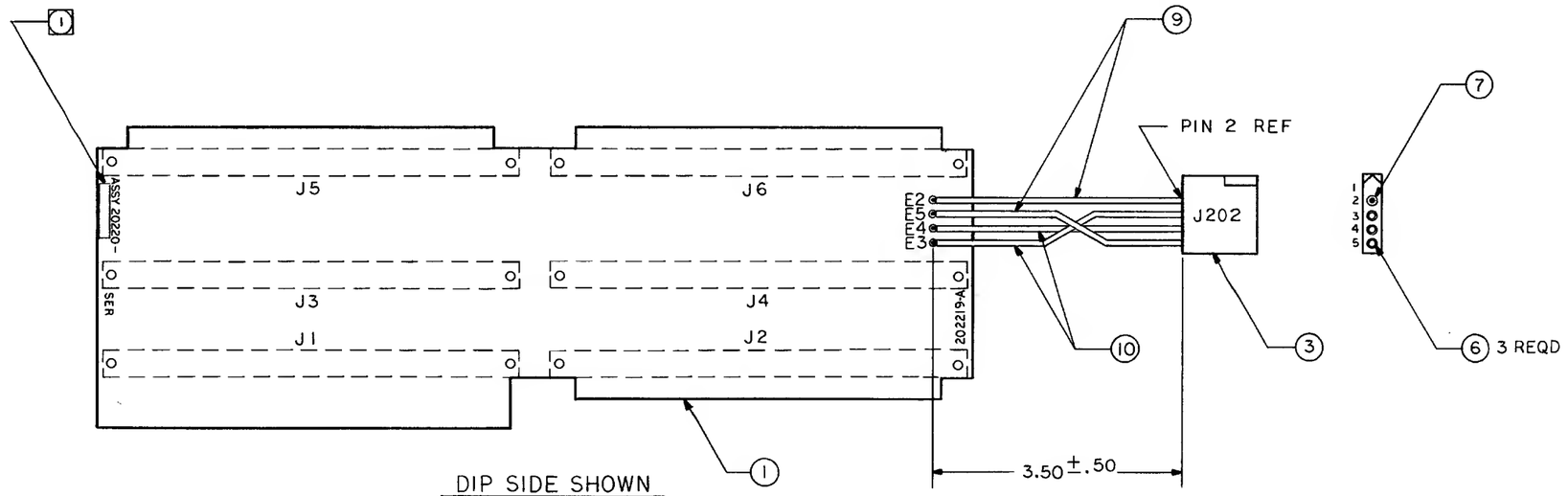
DATE 6/30/75

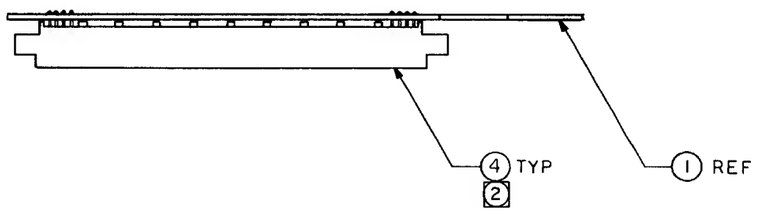
APPROVED

ITEM NO.	DESCRIPTION	PART NO.	REQD	MATL REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
	USE MATERIAL LIST AND ADD/DELETE THE FOLLOWING:-	201659-000		H		200685
1	Wire, Solid, Insulated.	100333-930	A/R			Jumper E601 to E602 Add.
						E613 to E614 Add.
						E618 to E619 Add.
						E623 to E624 Add.
						E629 to E630 Add.

FORM 209 (R.12/74)

REVISIONS				202220 A
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	PILOT REL	JK	10/11/74	D. Aspinwall
A	MFG RELEASE NO CHG	JK	12/4/75	[illegible]





2 SEE M/L (DASH VERSIONS) FOR QTY. AND LOCATIONS OF CONNECTORS TO BE INSTALLED.

1 MARK LATEST ASSY. LEVEL, APPROPRIATE DASH NO. AND SER. NO.
.12 HIGH WHITE CHARACTERS PER WANGCO SPEC. 100037.

NOTES: UNLESS OTHERWISE SPECIFIED.

PART NO. 202202-XXX SEE TABULATED M/L.

NOTES UNLESS SPECIFIED 1. TOLERANCES .XX± ANGULAR .XXX± ± 2. BREAK ALL SHARP EDGES APPROX. .01D 3. MACH. SURFACES √ 4. ALL DIMS IN INCHES.	DRAWN [illegible] 10-74 CHECK APPR. D. Aspinwall 10/11/74 MATERIAL FINISH MODEL No. FORMATTER W/ EMUL NEXT ASSY 202221 202222, 202223	Wangco Incorporated ASSEMBLY, PWB REAR CONNECTOR PANEL CODE F 120 QTY. REQ'D. 1 SCALE 1:1 SIZE D 202220 A DO NOT SCALE THIS DRAWING WEIGHT SHEET 2 OF 2	

REV. A

PART NUMBER 202220-000

DATE

APPROVED

WANGCO INCORPORATED

MATERIAL LIST

CODE
F120

PART NUMBER	REV.
202220-000	A

TITLE ASSY. PWB REAR CONNECTOR PANEL. MODEL FORMATTER DATE 1/13/75 SHEET 1 OF 2

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
1	Board, Processed.	202219-001	1	A		
2						
3	Connector, 5 Pin.	100010-005	1			J202
4	Connector, 100 Pin.	100355				See Build M/L for Qty.
5						
6	Pin, Connector - Female	100021-006	3			
7	Pin, Connector - Male.	" -007	1			
8						
9	Wire, 14GA, White	100053-914	A/R			
10	Wire, 18GA, White	" -918	A/R			
11						
12						
13						
14	Printed Master	202218	Ref.			

WANGCO INCORPORATED

MATERIAL LIST

CODE 120

PART NUMBER	REV.
202220-001	A

TITLE ASSY. PWB REAR CONNECTOR PANEL. MODEL 511 DATE 10/2/74 SHEET 1 OF 1

PART NUMBER 202220-001 REV. A

APPROVED DATE 10/15/74

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD THE FOLLOWING:-	202220-000		A		NEXT ASSEMBLY/USED ON 202222-000
4	Connector, 100 Pin.	100355	2			J5, J6.

REV. A

PART NUMBER 202220-002

APPROVED

DATE 10/2-74

WANGCO INCORPORATED

MATERIAL LIST

CODE
80120

PART NUMBER	REV.
202220-002	A

TITLE ASSY. PWB. REAR CONNECTOR PANEL. MODEL 512 DATE 10/2/74 SHEET 1 OF 1

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD THE FOLLOWING:-	202220-000		A		NEXT ASSEMBLY/USED ON: 202223-000
4	Connector, 100 Pin.	100355	4			J3, 4, 5, 6,

REV. A

PART NUMBER 202220-003

DATE 10/2/74

APPROVED

WANGCO INCORPORATED

MATERIAL LIST

CODE
120

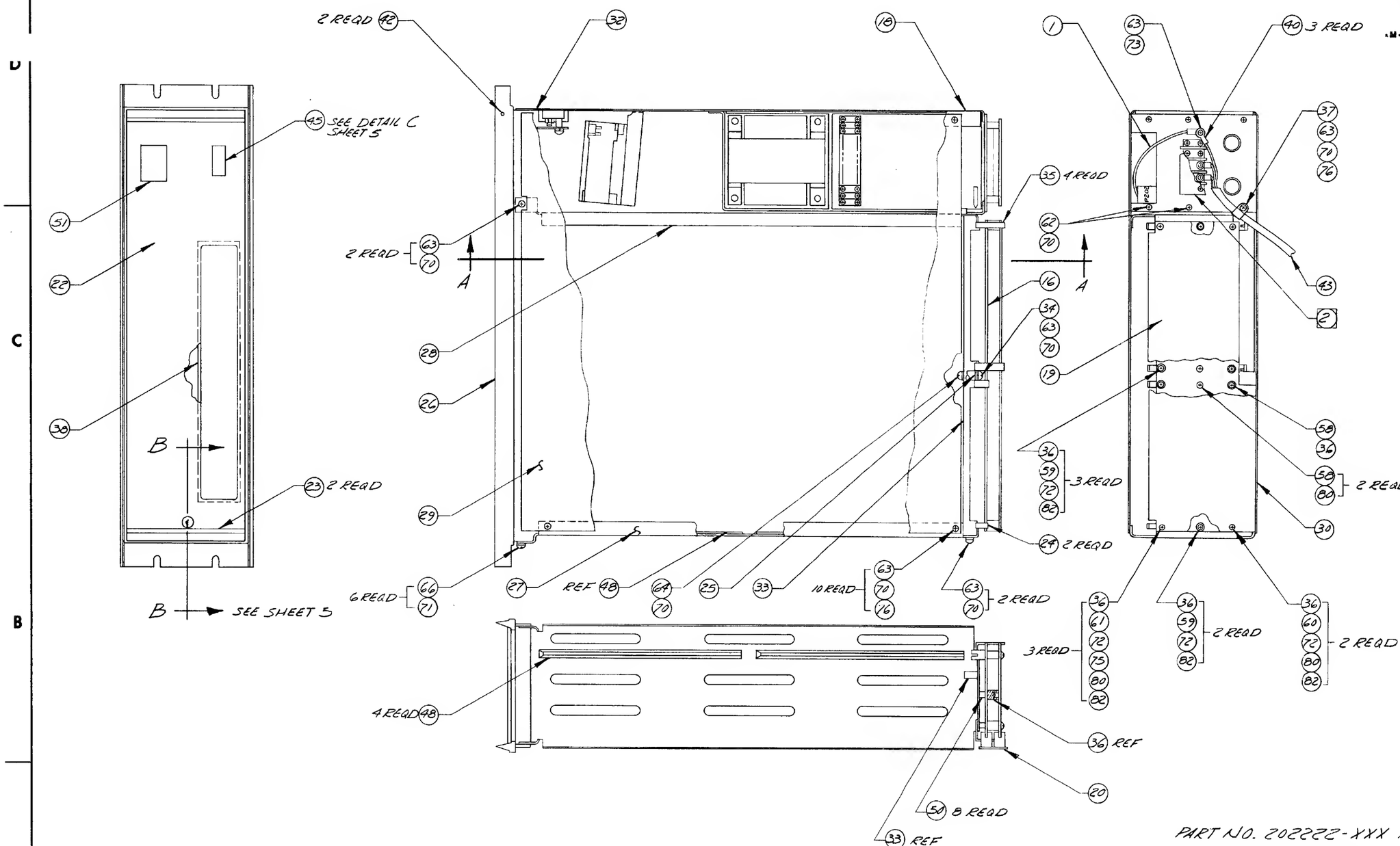
PART NUMBER	REV.
202220-003	A

TITLE ASSY. PWB. REAR CONNECTOR PANEL. MODEL 513 DATE 10/2/74 SHEET 1 OF 1

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
	USE MATERIAL LIST AND ADD THE FOLLOWING:-	202220-000		A		NEXT ASSEMBLY/USED ON 202221-000
4	Connector, 100 Pin.	100355	6			J1,2,3,4,5,6,

FORM 209 (R.12/74)

REVISIONS				202222 D
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG RELEASE		12/11/74	R. SERPICO
B	CR/O 4559	TB	4/29/75	TB
C	CR/O 4610	TB	12/17/75	TB
D	CR10 5737	TB	8/6/75	KS



SECTION A-A
TOP & BOTTOM COVER REMOVED FOR CLARITY

PART NO. 202222-XXX ASSY SEE TABULATED M/L

(2) APPLY VOLTAGE MARKER AS READ
~~(7) RUBBER STAMP FUSE VALUE WHERE SHOWN.~~
NOTES: UNLESS OTHERWISE SPECIFIED.

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± — ANGULAR .XXX± — ± —	DRAWN	LECAND	1-9-75
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.	R. SERPICO	10-10-74
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER 511	
	NEXT ASSY		

Wangco Incorporated

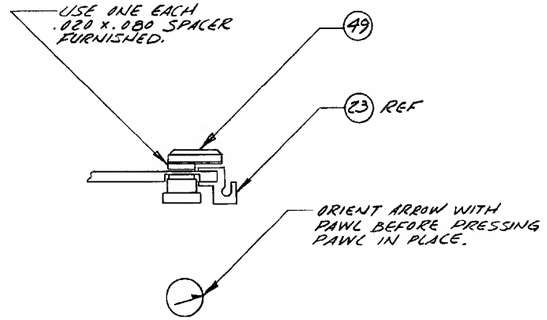
ASSY, NREI FORMATTER WITH TYPE 'P' EMULATOR

CODE ID 101 | QTY. REQ'D. 1

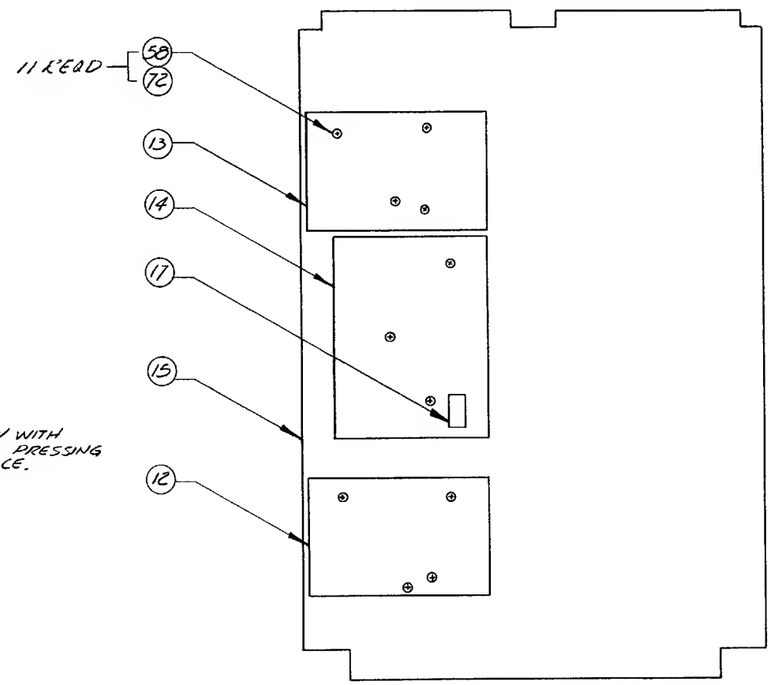
SCALE 1/2 & NOTED | SIZE D | 202222 CHARTED | D

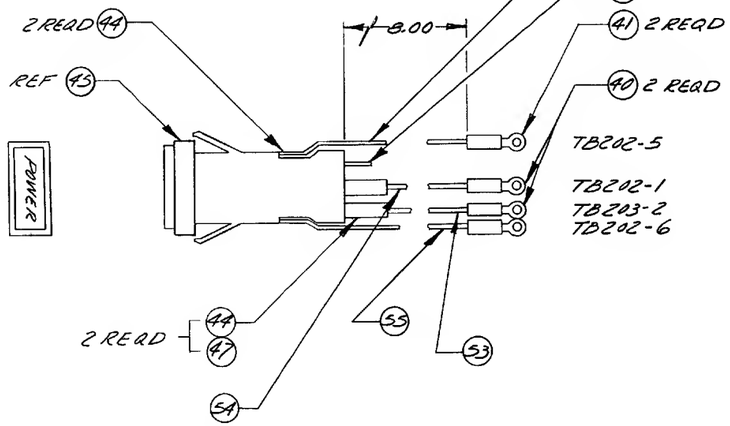
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 4 OF 5

REVISIONS				202222
REV.	DESCRIPTION	CHK.	DATE	APPROVED
—	SEE SHEET 4	—	—	——



SECTION B-B
THRU DOOR ONLY
SCALE: FULL, ROTATED 90°





DETAIL C
SCALE: 1/1

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN		1-9-75
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No. FORMATTER 511		
	NEXT ASSY		

Wangco Incorporated

ASSY, NRZI FORMATTER WITH TYPE 'P' EMULATOR

CODE F01 | QTY REQ'D. 1

SCALE 1/2 & NOTED | SIZE D | 202222 CHARTED | D

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 5 OF 5

B-57

202222

CODE
F101

PART NUMBER	REV.
202222-000	D

WANGCO INCORPORATED

MATERIAL LIST

TITLE ASSY. NRZI FORMATTER. WITH TYPE "P" EMULATOR. MODEL 511 DATE 6/19/75 SHEET 1 OF 5

REV.	D
PART NUMBER	202222-000
DATE	
APPROVED	

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
1	Assy. Jumper.	200289-001	1			
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12	Assy. Delay Counter Pwb.	201650-XXX	1			See build M/L for dash no.
13	Assy. CRC Generator Pwb.	201653-001	1			
14	Assy. Clock Generator Pwb.	201656-001	1			
15	Assy. NRZI Control Pwb.	201659-XXX	1			See build M/L for dash no.
16	Assy. Rear Connector Panel.	202220-001	1			
17	Assy. Speed Chip.		1			See build M/L for part no.
18	Assy. Power Supply.	201581-XXX	1			See build M/L for dash no.
19	Assy. Emulator Pwb.	202233-001	1			
20	Assy. Emulator Interface. PWB.	202202-001	1			
21	Assy. Cable-MTU	201336-060	1			
22	Door, Formatter.	201245-XXX	1			See build M/L for dash no.
23	Trim, Panel.	201243-001	2			
24	Bracket, Connector Support.	202139-001	2			
25	Strap, Connector Support.	201252-001	1			
26	Casting, Front Panel.	201255-XXX	1			See build M/L for dash no.
27	Support, Right Hand.	201287-001	1			
28	Support, Center.	201288-001	1			
29	Cover, Top.	201320-001	1			
30	Cover, Bottom.	201320-002	1			
31	Kit, Ship Away.	202196-XXX	1			See build M/L for dash no.
32	Label, Model.	201347-001	1			
		B-59				

REV. D | PART NUMBER 202222-000 | DATE | APPROVED

WANGCO INCORPORATED

MATERIAL LIST

CODE F101

PART NUMBER	REV.
202222-000	D

TITLE ASSY. NRZI FORMATTER WITH TYPE "P" EMULATOR. MODEL 511 DATE 6/19/75 SHEET 2 OF 5

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
33	Stiffener, Connector Panel.	201384-001	1			
34	Pin, Guide.	201538-001	1			
35	Support, Conn.	202217-001	4			
36	Spacer.	202216-001	10			
37	Clamp, Cable.	100000-003	1			
38	Tape, Adhesive Sealing.	100002-002	A/R			
39						
40	Terminal, Ins. Ring Tongue.	100057-004	5			
41	Terminal, " " "	100058-004	2			
42	Pin, Dowel.	100045-314	2			1/8 x ½"
43	Cord, AC Power.	100076-001	1			
44	Terminal, Quick Disconnect.	100139-002	4			
45	Switch & Indicator.	100179-001	1			S1.
46	Tubing, Thermofit.	100185-004	A/R			
47	Insulator.	100232-001	2			Use with item 44.
48	Guide, Card.	100326-001	4			
49	Latch, Arrowhead.	100357-001	1			
50	Spacer, Fibre.	100391-001	8			
51	Nameplate "W" Logo.	200034-001	1			
52	Wire, Insulated.	100053-124	A/R			Brown
53	Wire, "	-318	A/R			Orange.
54	Wire, "	-418	A/R			Yellow.
55	Wire, "	-524	A/R			Green.
56						
57	Screw, Pan Head.	100036-204	11			4-40 x 1/4"
58	Screw, " "	-210	3			4-40 x 5/8"
59	Screw, " "	-216	5			4-40 x 1"
60	Screw, " "	-220	1			4-40 x 1¼"
61	Screw, " "	-224	3			4-40 x 1½"
62	Screw, " "	-305	2			6-32 x 5/16"
63	Screw, " "	-306	17			6-32 x 3/8"
64	Screw, " "	-312	1			6-32 x 3/4"
		B-60				

CODE F101

WANGCO INCORPORATED

MATERIAL LIST

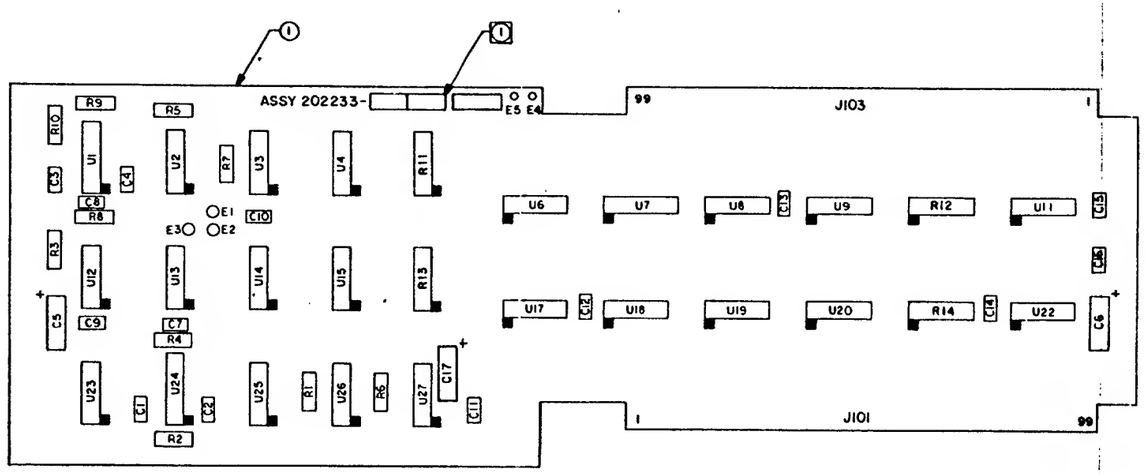
PART NUMBER	REV.
202222-000	D

TITLE ASSY. NRZI FORMATTER WITH TYPE "P" EMULATOR. MODEL 511 DATE 6/19/75 SHEET 3 OF 5

REV. D | PART NUMBER 202222-000 | DATE | APPROVED

ITEM NO.	DESCRIPTION	PART NO.	REQD	MIN. REV.	ACT. REV.	REMARKS
						NEXT ASSEMBLY/USED ON
65						
66	Screw,Pan Head.	100036-405	6			8-32 x 5/16"
67						
68						
69	Washer, Split Lock.	100042-200	12			No.4.
70	Washer, " "	-300	19			No.6.
71	Washer, " "	-400	6			No.8.
72	Washer, Lock Int. Tooth.	100059-200	20			No.4.
73	Washer, " " "	-300	1			No.6.
74						
75	Washer, Flat.	100047-200	3			No.4.
76	Washer, "	-300	11			No.6.
77						
78						
79						
80	Washer, Flat Nylon.	100050-100	6			No.4.
81						
82	Nut, Hex.	100043-200	9			4-40.
83						
84						
85						
86	Test Procedure, Run-Up.	201602	Ref.			
87	Test Procedure, Datum System.	201603	Ref.			
88	Logic Schematics, Form NRZI	200452	Ref.			
89						
90	Block Diagram, Formatter NRZI	200670	Ref.			
91	Schematic Emulator.	202193	Ref.			
		B-61				

IC'S				CAPACITOR		RESISTORS	
REF	ZONE	REF	ZONE	REF	ZONE	REF	ZONE
U1	E7	U18	E4	C1	D6	R1	D6
U2	E6	U19	E4	C2	D6	R2	D6
U3	E6	U20	E4	C3	E7	R3	E7
U4	E6			C4	E7	R4	D6
		U22	E3	C5	D7	R5	F6
U6	E5	U23	D7	C6	D3	R6	D6
U7	E4	U24	D6	C7	E6	R7	E6
U8	E4	U25	D6	C8	E7	R8	E7
U9	E4	U26	D6	C9	D7	R9	F7
		U27	D5	C10	E6	R10	F7
U11	E3			C11	D5	R11	E5
U12	E7			C12	E5	R12	E3
U13	E6			C13	E4	R13	E5
U14	E6			C14	E3	R14	E3
U15	E6			C15	E3		
				C16	E3		
U17	E5			C17	D5		



2. FOR SCHEMATIC REF DWG SEE 202234.

(1) MARK APPROPRIATE DASH NO.S (LATEST REVISION LETTERS WHERE SHOWN. 12 HIGH CHARACTERS, COLOR WHITE PER WANGCO SPEC 100D37.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	REVISIONS DESCRIPTION	DWN	DATE	202233 E APPROVED
A	PILOT RELEASE			
B	SEE CR/O 4425			
E	CR/O 7228			

PART NUMBER 202233-001 ASSY

Wangco Incorporated

ASSEMBLY, PWB
EMULATOR
TYPE 'P'

SCALE	SIZE	
2:1	202233	E

SHEET 3 OF 3

B-63

202233 3 OF 3
ASSEMBLY PWB, EMULATOR TYPE 'P'

WANGCO INCORPORATED

MATERIAL LIST

ML

DRAWING NO.	REV.
202233-001	E

DRAWING TITLE ASSY. PWB EMULATOR. MODEL NO. Type 'P' DATE 10/2/74 SHEET 1 OF 3

DRAWING NO. 202233-001 REV. E

ML

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
1	Process Board, Emul. Type 'P'	202232-001	E	1	
2					
3					
4	IC 7407	100327-001		4	U4,9,19,20.
5	IC 7404	100330-001		5	U14,17,18,25,27.
6	IC 7406	100331-001		3	U2,6,22.
7	IC 7410	100333-001		1	U13.
8	IC 7438	100336-001		5	U3,U8,U7 ,12,26.
9	IC 7474	100339-001		1	U15.
10	IC 7475	100340-001		1	U11.
11	IC 9602	100234-001		2	U1,24.
12	IC 74107	101014-001		1	U23.
13					
14					
15					
16					
17	Resistor Network 220	142003-221		2	R13,14.
18	Resistor, " 330	" -331		2	R11,12.
19	Resistor, 5%,¼W. 1K	100156-102		5	R1,3,5,6,7.
20	Resistor, " " 2K	" -202		1	R10.
21	Resistor, " " 20K	" -203		4	R2,4,8,9.
22					
23					
24					
25					
26	Capacitor Tant. 4.7uf	100363-475		3	C5,6,17.
27	Capacitor Cer. 0.1uf	100364-104		10	C7 - 16.
28	Capacitor Sil. Mica 150pf	100243-151		3	C2,3,4.
29	Capacitor, " " 20pf	" -200		1	C1.
30					
31					
32					

FORM 209 (5/74)

3-24-77

REV. E

DRAWING NO. 202233-001

ML

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202233-001 | REV. E

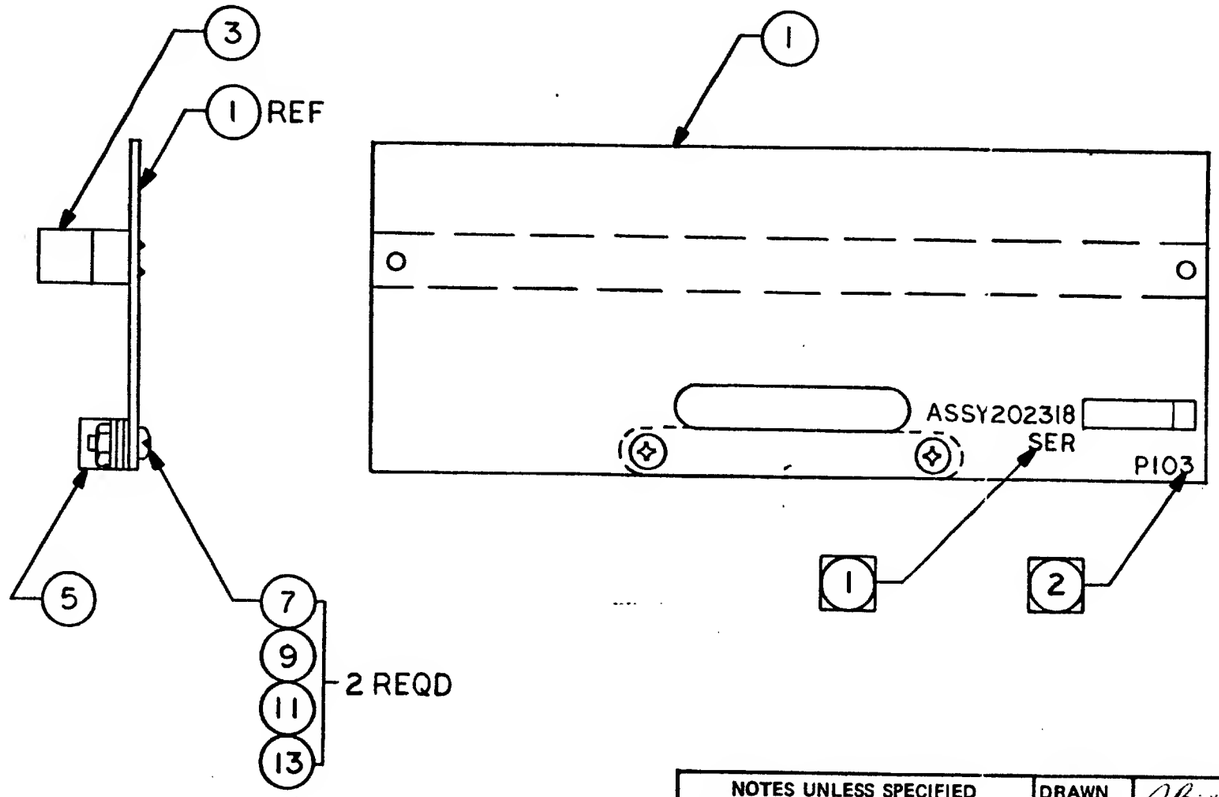
DRAWING TITLE ASSY. PWB EMULATOR. MODEL NO. Type 'P' DATE 10/2/74 SHEET 2 OF 3

Item No.	Drawing Title	Dwg. No.	Rev.	Qty.	Remarks on Ckt. Desig.
33					
34	Wire Wrap Pin (jumper)	100360-001		3	E1,2,3
35					
36	Wire, Solid, 30 AWG	100383-930		A/R	Jumper E2 to E3.
37					
38					
39	Printed Master.	202231-001	D	0	
40	Schematic.	202234-001	C	0	
	Rework Instructions.	500271-001		0	

3-24-77

FORM 209 (5/74)

REVISIONS				202318 A
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	MFG RELEASE	PB	12/5/74	



[2] RUBBER STAMP REF DESIGNATION .12HIGH WHITE CHARACTERS.

[1] MARK ASSY LATEST REVISION LETTER AND S/N .12HIGH WHITE CHARACTERS PER WANGCO SPEC 100037.

NOTES: UNLESS OTHERWISE SPECIFIED

PART NUMBER 202318-001 ASSY

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR ±, .XXX±	DRAWN	J Brady	12-6-74
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.	[illegible]	12-6-74
4. ALL DIMS IN INCHES.	MATERIAL	—	
	FINISH	—	
	MODEL No.	FORMATTER TYPE 'P' EMULATOR	
	NEXT ASSY	202196	

Wangco Incorporated

ASSEMBLY, CABLE BOARD - INPUT/OUTPUT

CODE	QTY. REQ'D.
F120	

SCALE	SIZE		
—	B	202318	A
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 2 OF 2	

F120

WANGCO INCORPORATED

MATERIAL LIST

ML | DRAWING NO. 202318 001 | REV. A

DRAWING TITLE: ASSY. CABLE BOARD INPUT/OUTPUT. FORMATTER TYPE 'P' EMULATOR

MODEL NO. | DATE 12/2/74 | SHEET 1 OF 2

ITEM NO.	DRAWING TITLE	DWG. NO.	NO. REQ.	REMARKS ON CKT. DESIG.
1	Board, Processed	202317	1	REV 'A'
2				
3	Connector 100 pin	100355	1	
4				
5	Clamp, Cable	100000-006	1	
6				
7	Screw, P. H.	100036-306	2	6-32 x 3/8"
8				
9	Washer, Split Lock	100042-300	2	No. 6
10				
11	Nut, Hex.	100043-300	2	6-32
12				
13	Washer, Flat	100047-300	2	No. 6
14				
15				
16	Printed Master.	202316	Ref	REV 'A'

APPENDIX C
MODEL 511 NRZI MAGNETIC TAPE FORMATTER
LOGIC SCHEMATICS AND WIRE LIST INDEX

This appendix contains the circuit schematics and the wiring diagrams for all assemblies and sub-assemblies in the Model 511 NRZI Formatter.

The circuit schematics are complete representations of the electronic circuitry. The user of this manual may want to consult the schematics in conjunction with his study of the text and the simplified circuit diagrams in the text sections. These documents are identified in the following list.

APPENDIX C
MODEL 511 NRZI MAGNETIC TAPE FORMATTER
LOGIC SCHEMATICS AND WIRE LIST INDEX

REVISIONS				
REV.	DESCRIPTION	CHK	DATE	APPROVED
A	MFG RELEASE			
B	SEE CR/O 3001			
C	SEE CR/O 3997			
D	CR/O 6088			
E	CR/O 6197			
F	CR/O 6275		11/7/74	C.S.

R406 10K
R405 10K
C406 .047UF
C407 N.U.
C405 .047UF
C411 2200PF
R404 1K
XC401 180.0 KHZ
F800
VLD
SPDCLK
SPDCLK
5V1
S16
VLD
SPD CLK
SPD CLK
TAPE SPEED CLOCK GENERATOR

R407 10K
R408 10K
C408 .047UF
C408 N.U.
C410 .047UF
C412 3300PF
R409 1K
F556
XC402 125.1 KHZ
+5V
C401 C402 C403 C404

WCLK
WCLK
5V1
S16
WRC
WCLP
F800
800
F556
556
F200
200
WRC
WRITE CLOCK GENERATOR

R403 560
+5V
5V1

D5

PIN	TERM
1	VLD
2	SELECT B
3	WRP
4	
5	WCLP
6	SELECT D
7	GND
8	9 TRK
9	SELECT C
10	DDS
11	SPDCLK
12	F800
13	SELECT A
14	+5V

NOTES UNLESS SPECIFIED
1. TOLERANCES XX± ANGULAR XXX± ±
2. BREAK ALL SHARP EDGES APPROX. .010
3. MACH. SURFACES
4. ALL DIMS IN INCHES.

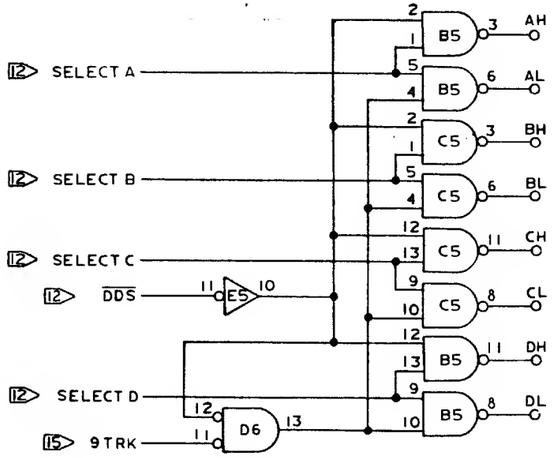
DRAWN L. ARCHER 4-8-73
CHECK
APPR.
MATERIAL
FINISH
MODEL No.
NEXT ASSY

Wangco Incorporated

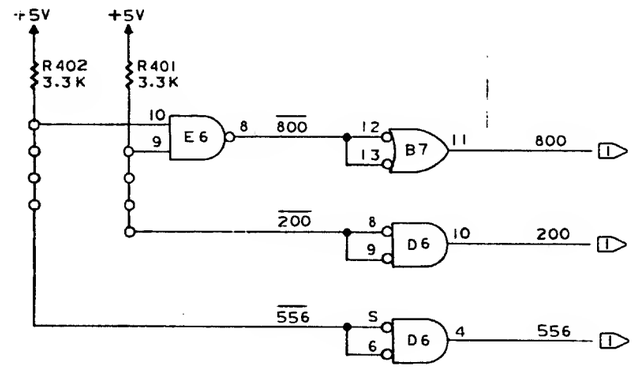
LOGIC SCHEMATIC
NRZI FORMATTER
(CLOCK GENERATOR)

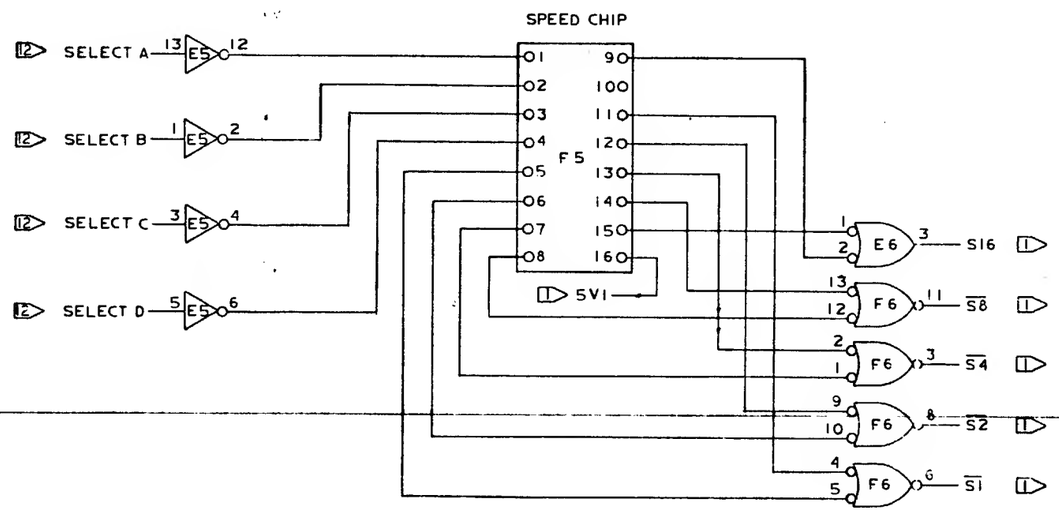
CODE IDENT NO. 10098
QTY. REQ'D.
SCALE
SIZE D
200452
F
DO NOT SCALE THIS DRAWING
WEIGHT
SHEET 1 OF 15

REVISIONS				
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			



7-TRACK DENSITY SELECTION





TAPE SPEED SELECTION

NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR XXX± ±	DRAWN	L. AGUIRRE	4-6-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(CLOCK GENERATOR)

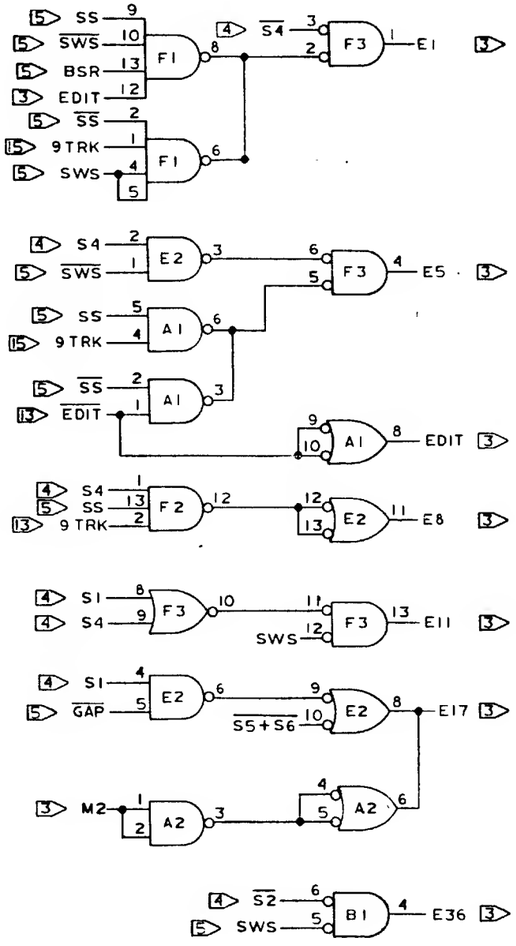
CODE F 108 | QTY REQ'D.

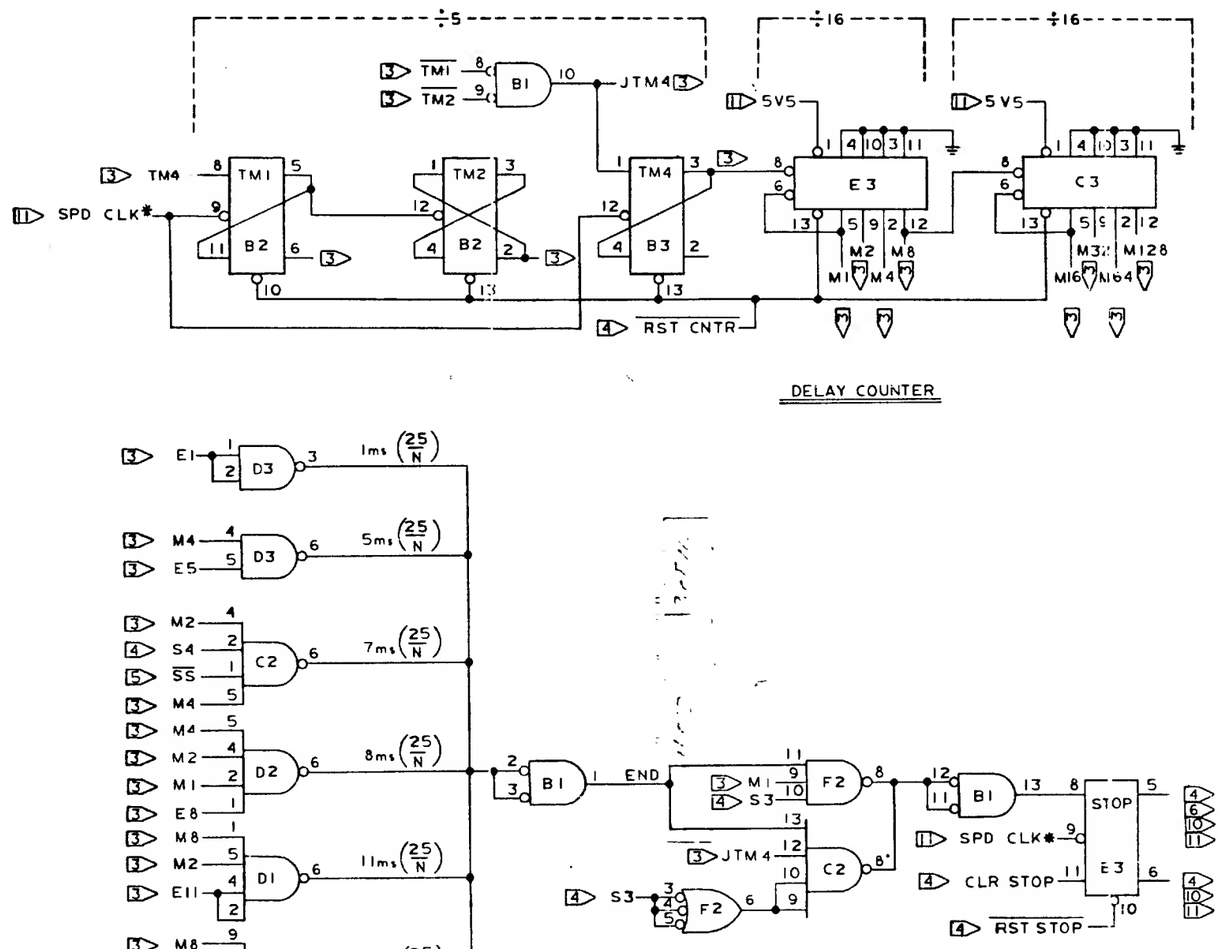
SCALE | SIZE D | 200452 | F

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 2 OF 16

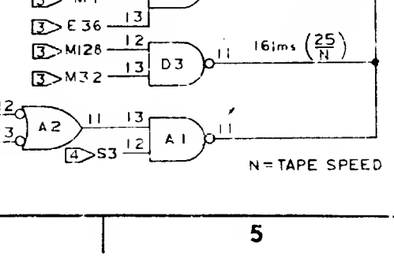
LOGIC SCHEMATIC NRZI FORMATTER

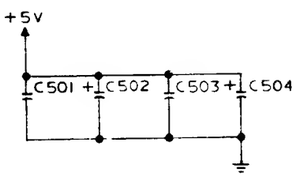
REVISIONS					200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED	
	SEE SHT 1				

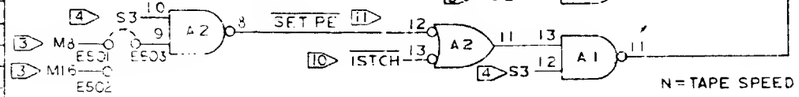




DELAY COUNTER







C1

PIN	TERM
1	5V5
2	EDIT
3	$\overline{SS}$
4	$\overline{SET\ PE}$
5	STOP
6	$\overline{RST\ CNTR}$
7	GND
8	CLR STOP
9	$\overline{RST\ STOP}$
10	$\overline{S2}$
11	$\overline{STOP}$
12	9TRK
13	SPD CLK*
14	+5V

E1

PIN	TERM
1	BSR
2	$\overline{SS}$
3	S4
4	SWS
5	$\overline{SWS}$
6	SS
7	GND
8	$\overline{S5+S6}$
9	$\overline{ISTCH}$
10	$\overline{S4}$
11	$\overline{S3}$
12	$\overline{GAP}$
13	S1
14	+5V

NOTES UNLESS SPECIFIED
1. TOLERANCES XX± ANGULAR XXX± ±
2. BREAK ALL SHARP EDGES APPROX. .010
3. MACH. SURFACES ✓
4. ALL DIMS IN INCHES.

DRAWN L. AGUIRRE 4-9-73
CHECK
APPR
MATERIAL
FINISH
MODEL No.
NEXT ASSY

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(DELAY COUNTER)

CODE F 126 QTY REQ'D.

SCALE | SIZE D | 200452 | F

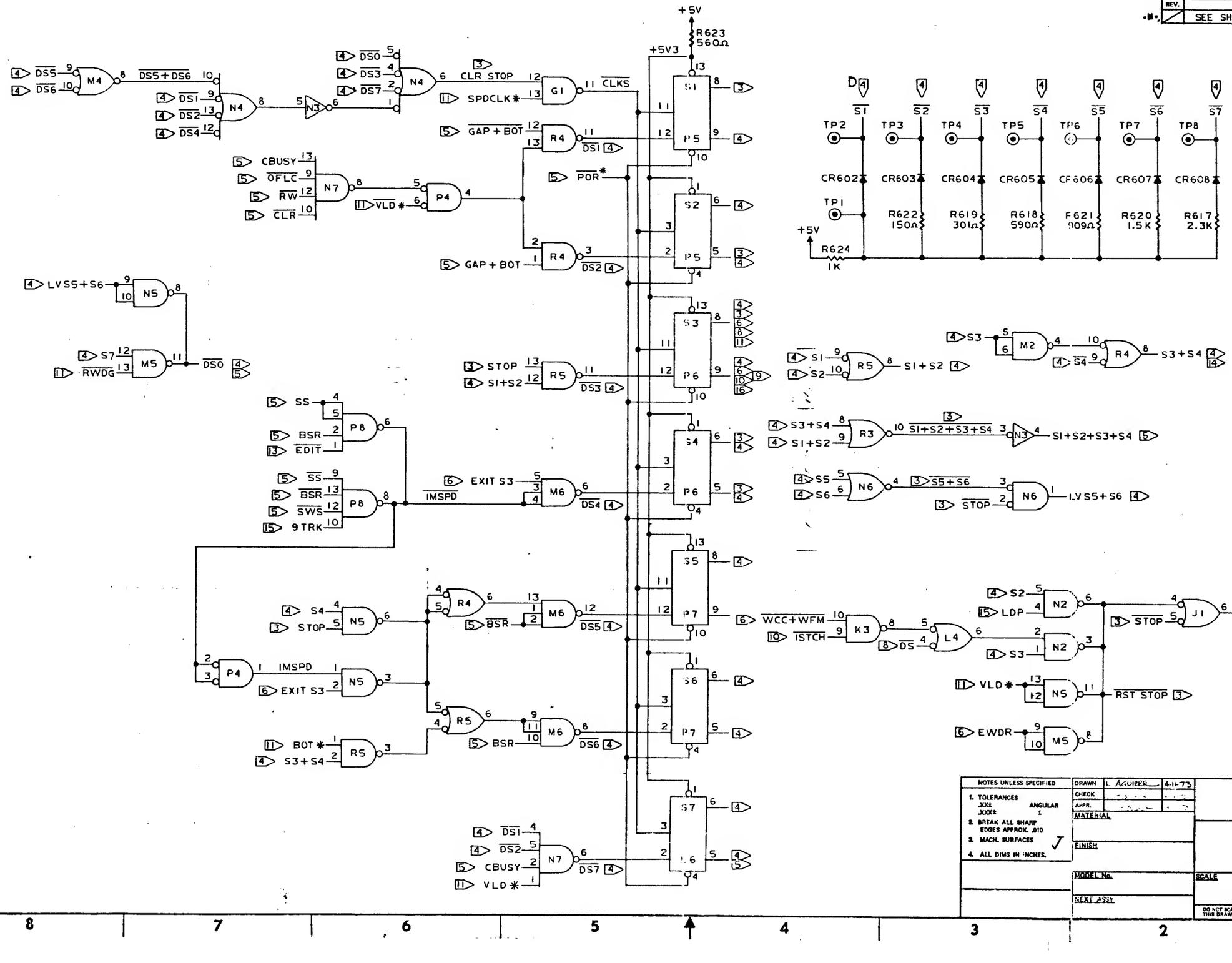
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 3 OF 16

3

LOGIC SCHEMATIC NRZI FORMATTER

REVISIONS				200452 F
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

LOGIC SCHEMATIC NRZI FORMATTER



NOTES UNLESS SPECIFIED	DRAWN	L. AGUIRRE	4-11-73
1. TOLERANCES .XX± ANGULAR .XXX± ±	CHECK		
2. BREAK ALL SHARP EDGES APPROX. .010	APPR.		
3. MACH. SURFACES ✓	MATERIAL		
4. ALL DIMS IN INCHES.	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(STATE COUNTER LOGIC)

CODE F 108 | QTY. REQ'D.

SCALE | SIZE D | 200452 | F

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 4 OF 16

C-11

REVISIONS				
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

SET WCC → WCC K8 → ADDR, J7 → WCC *

SET WFM → WFM K8 → ADDR, R3 → WFM *

SET GAP → GAP K8

SET RCC → RCC K8 → ADDR, J7 → RCC *

SET REV → BSR M8

SET CLR → CLR M8

SET REW → RW M8

VLD, M7 → RW M8

VLD, SET REW, LDP → K7 → REW L7

POR, RWDG → N8 → REW L7

VLD, SET OFL → K10 → CFLC L7

ONLINE

SET OFL, SET REW → E601 E602 JUMPER FOR NO INT ON REWIND

VLD, K10 → CBUSY L6

DSØ, S7 → M4 → CBUSY L6

POR → CBUSY L6

CBUSY → A8 → CBUSY *

SET WCC, SET WFM → K9

SET GAP, L8 → L9 → SET RJCT

GAP, LDP → P4 → GAP+BOT → P4 → GAP+BOT

BSR → M9 → SRC

S1+S2+S3+S4 → M9 → SFC

BSR → M9 → SFC

REW, VLD → M4 → OFLC → M9 → OFFC

REW, VLD → N8 → M9 → RWC

LDP → M9 → RWC

WCC+WFM, GAP → J1 → SWS

ADDR → F0 → SWS

+5V UNREG

ON LINE → J6

R633 20K, R632 10K, C641 39UF → H8

EXT RESET, ADDR → K7 → POR

POR → M7

VLD, POR → L9 → POR * → M7 → POR *

VLD → N8 → SRS

+5V, R629 3.3K → SS

SINGLE → E617 → L8 → SS

SELECT C → G7 → C → SS

SELECT B → G7 → B → SS

SELECT D → G7 → D → SS

SELECT A → G7 → A → SS

E603 JUMPER FOR SINGLE STACK TAPES

NOTES UNLESS SPECIFIED	DRAWN		4-12-73
1. TOLERANCES XX± ANGULAR, XXX± ±	CHECK		
2. BREAK ALL SHARP EDGES APPROX. .010	APPR.		
3. MACH. SURFACES ✓	MATERIAL		
4. ALL DIMS IN INCHES.	FINISH		
	MODEL NO.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(COMMAND REG. CBUSY, RESET)

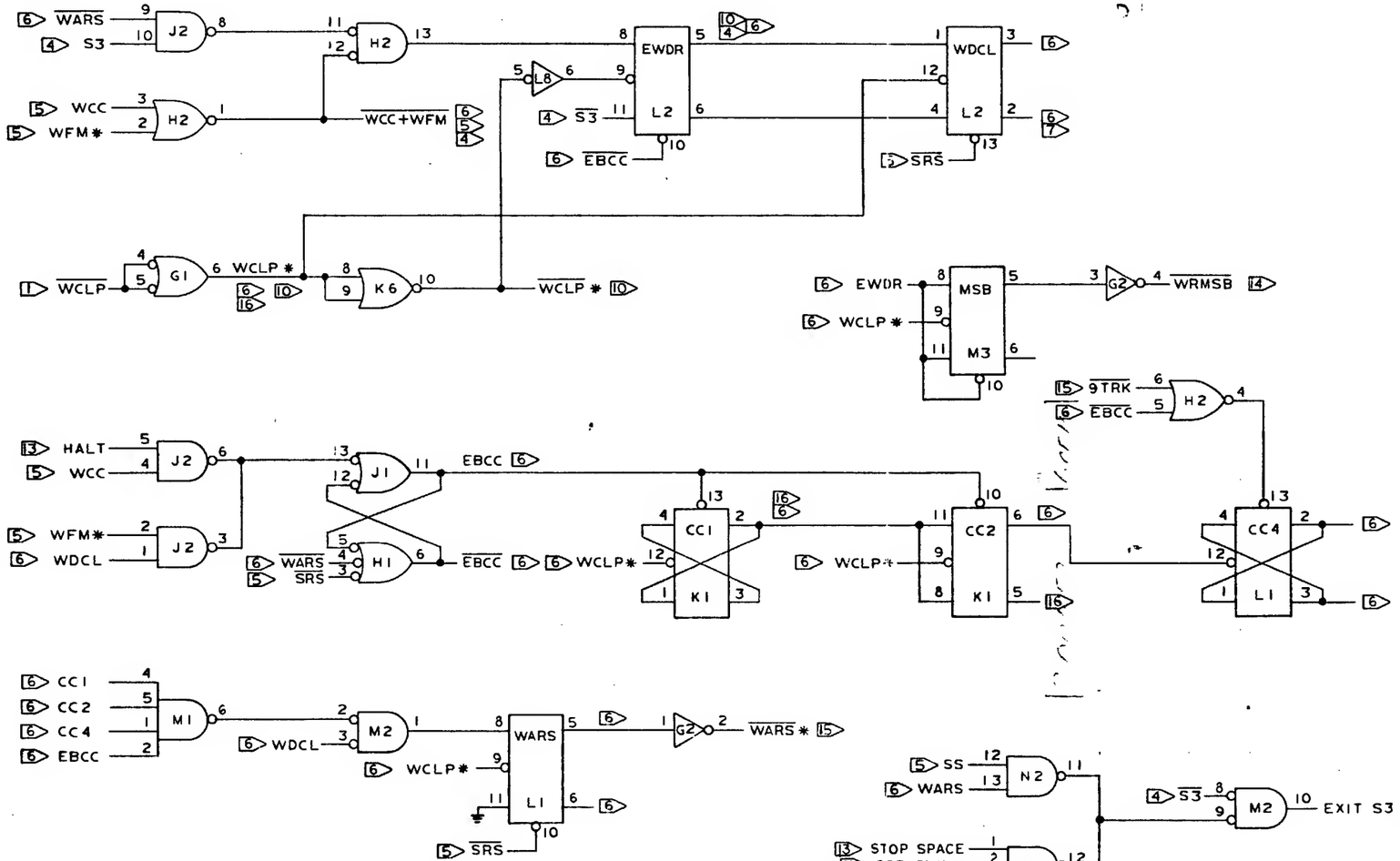
CODE F 103 QTY REQ'D.

SCALE | SIZE D | 200452 | F

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 5 OF 16

C-13

REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			



NOTES UNLESS SPECIFIED	DRAWN	L. AGUIRRE	4-12-73
1. TOLERANCES XX± ANGULAR, XXX± ±	CHECK		
2. BREAK ALL SHARP EDGES APPROX. .010	APPR		
3. MACH. SURFACES	MATERIAL		
4. ALL DIMS IN INCHES.	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(WRITE CONTROL LOGIC)

CODE F 108 | QTY. REQ'D.

SCALE | SIZE D | 200452 | F

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 6 OF 15

C-15

REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

LOGIC SCHEMATIC NRZI FORMATTER

H11: B0 B1 B2 B3 → CB0 CB0 CB1 CB1 CB2 CB2 CB3 CB3
R11: W/RACK → WRSTR
H12: B4 B5 B6 B7 → CB4 CB4 CB5 CB5 CB6 CB6 CB7 CB7

+5V, R630 3.3K
JUMPER TO WRITE 17 (OCTAL) FILE MARK IN 9 CH MODE.
CD, E608, E609, 9 TRK → L9
WFM*, 7 TRK + CD → K9

WDCL, WCC → G3
WDP → J9 → WDP
CB0 → G11 → WD0
CB1 → G11 → WD1
CB2 → G11 → WD2
CB3 → G11 → WD3
CB4 → G12 → WD4
CB5 → G12 → WD5
CB6 → G12 → WD6
CB7 → G12 → WD7

7 TRK + CD → A9
WFM* → A9
H9 inverters on WFM* lines

JUMPER TO DISABLE Q TO 12 CONVERSION
CB2 CB3 CB4 CB5 CB6 CB7 7EV → G10 → H10 → E623, E624

CB7 CB6 → J12
CB5 CB4 → J12
J12 J12 J12
CB3 CB2 → J11
CB1 CB0 → J11
ODD → N9

7ODD → J10 → WDP
7EV → J10
H10
9 TRK → K10
J11

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L. AGUIRRE	4-12-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES ✓	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(WRITE LOGIC)

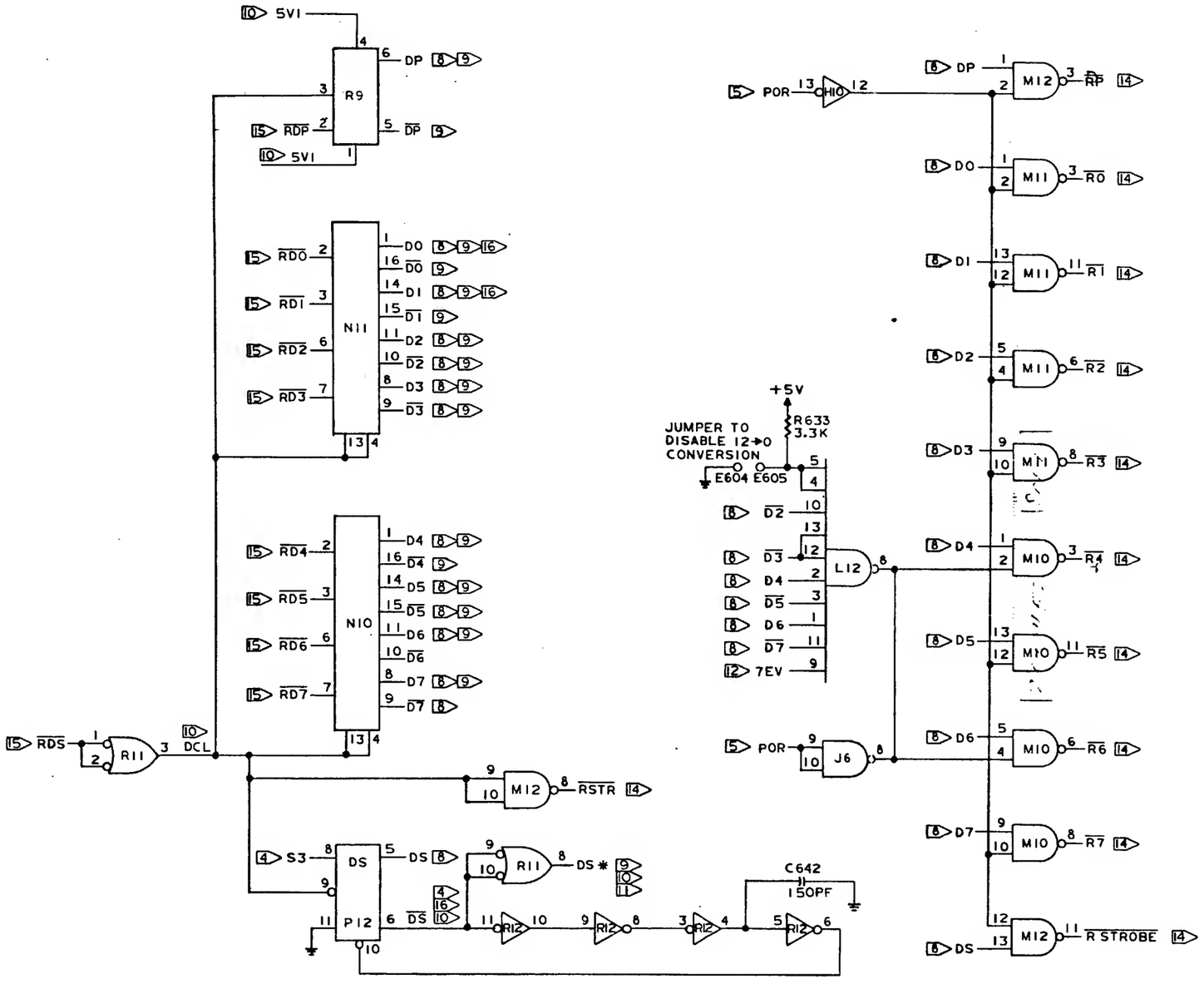
CODE F 106 — QTY. REQ'D.

SCALE — SIZE D — 200452 — F

DO NOT SCALE THIS DRAWING — WEIGHT — SHEET 7 OF 8

C-17

REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			



8

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L. AGUIRRE	4-16-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(READ REGISTERS)

CODE F 108 — ASY. REQ'D.

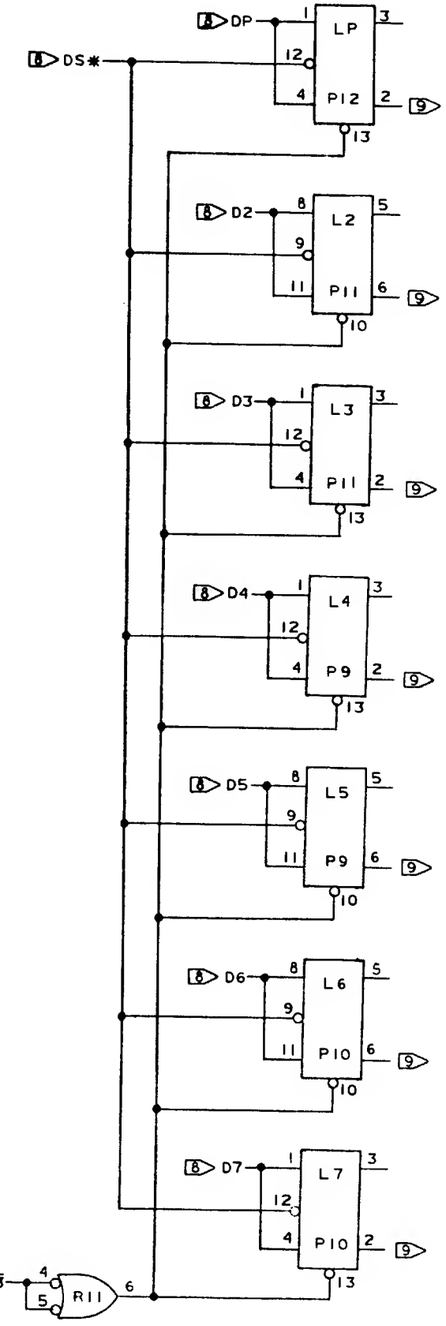
SCALE — SIZE D — 200452 — F

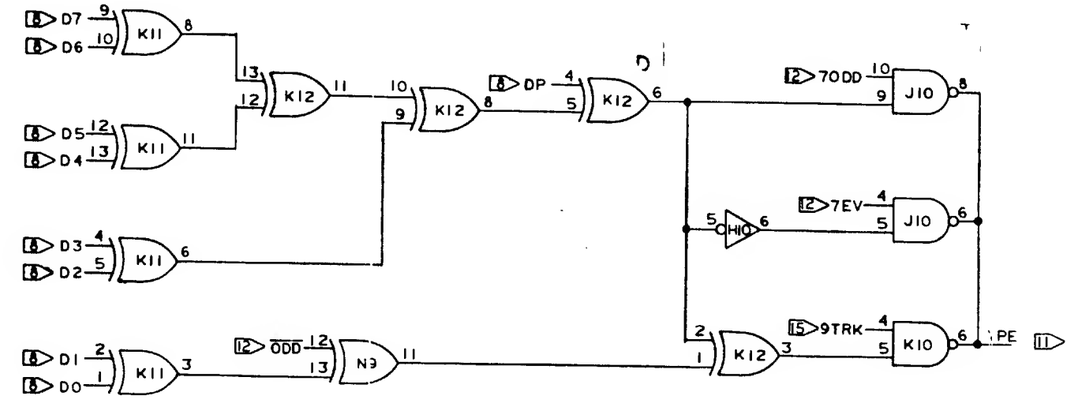
DO NOT SCALE THIS DRAWING — WEIGHT — SHEET 8 OF 16

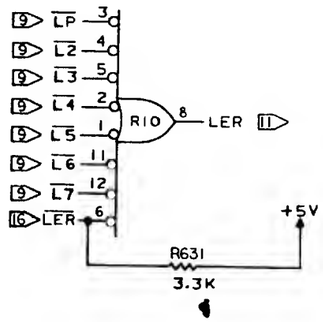
C-19

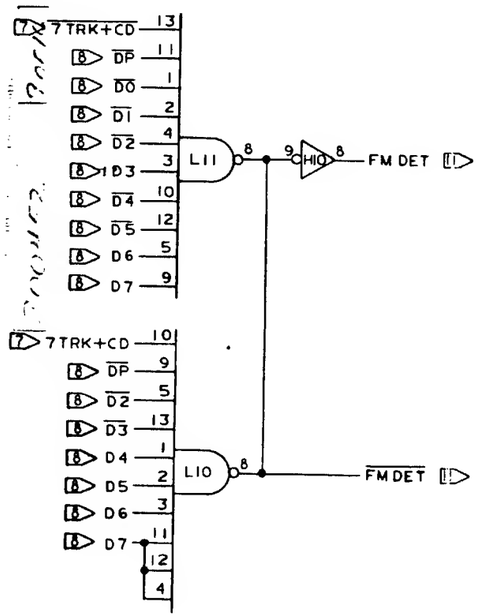
REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

LOGIC SCH NRZI Formatter









NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR XXX± ±	DRAWN	L. AGUIRRE	4-17-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES ✓	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(LRC, VPE, FM LOGIC)

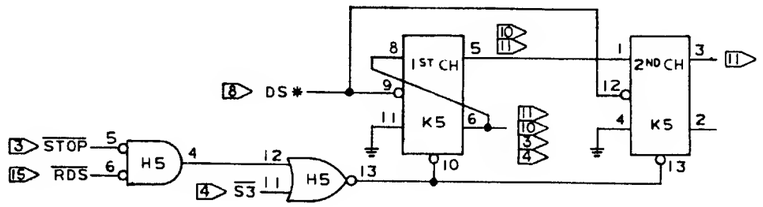
CODE F 100 | QTY. REQ'D.

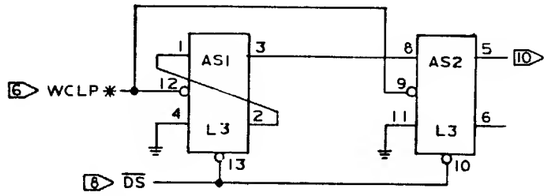
SCALE | SIZE D | 200452 | F

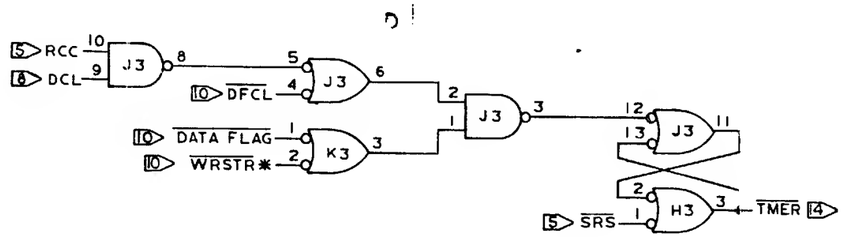
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 9 OF 16

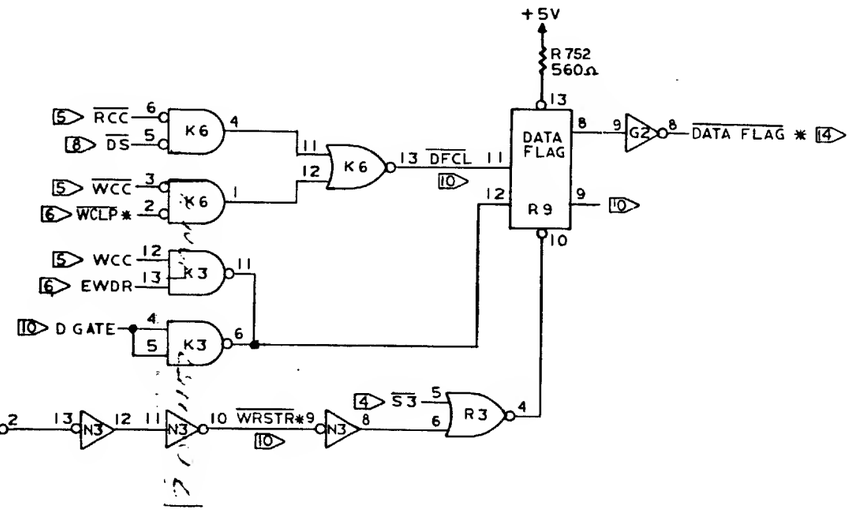
C-21

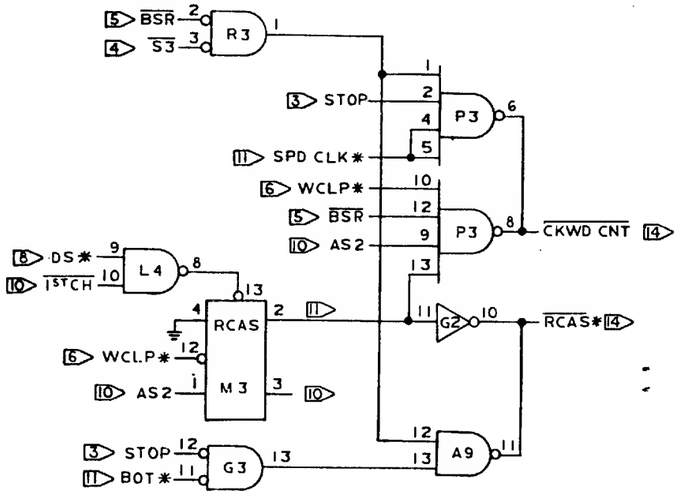
REVISIONS				200452 F
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

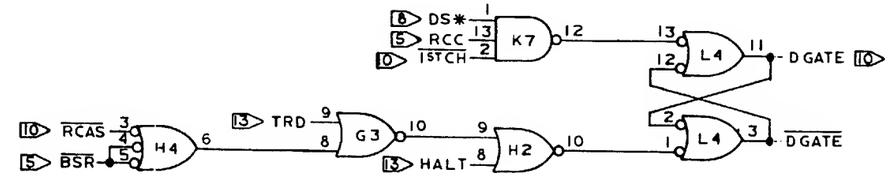












10

NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR .XXX± ±	DRAWN	L. AGUIRRE	4-17-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(READ CONTROL LOGIC)

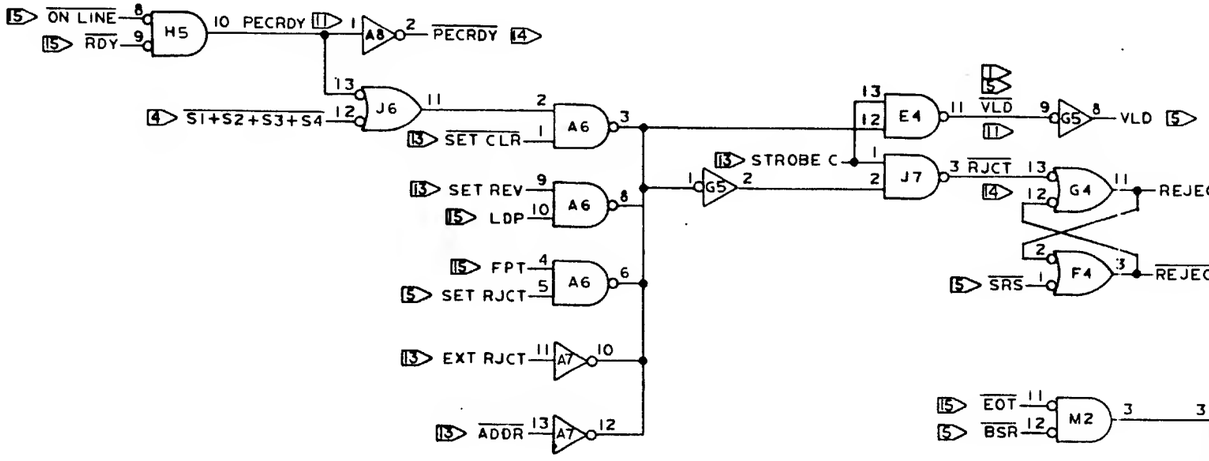
CODE F 108 | QTY REQ'D.

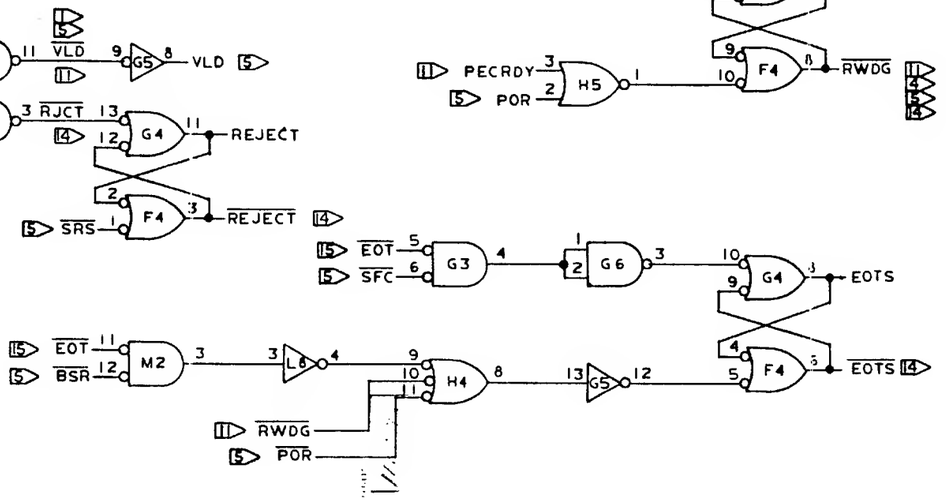
SCALE | SIZE D | 200452 | F

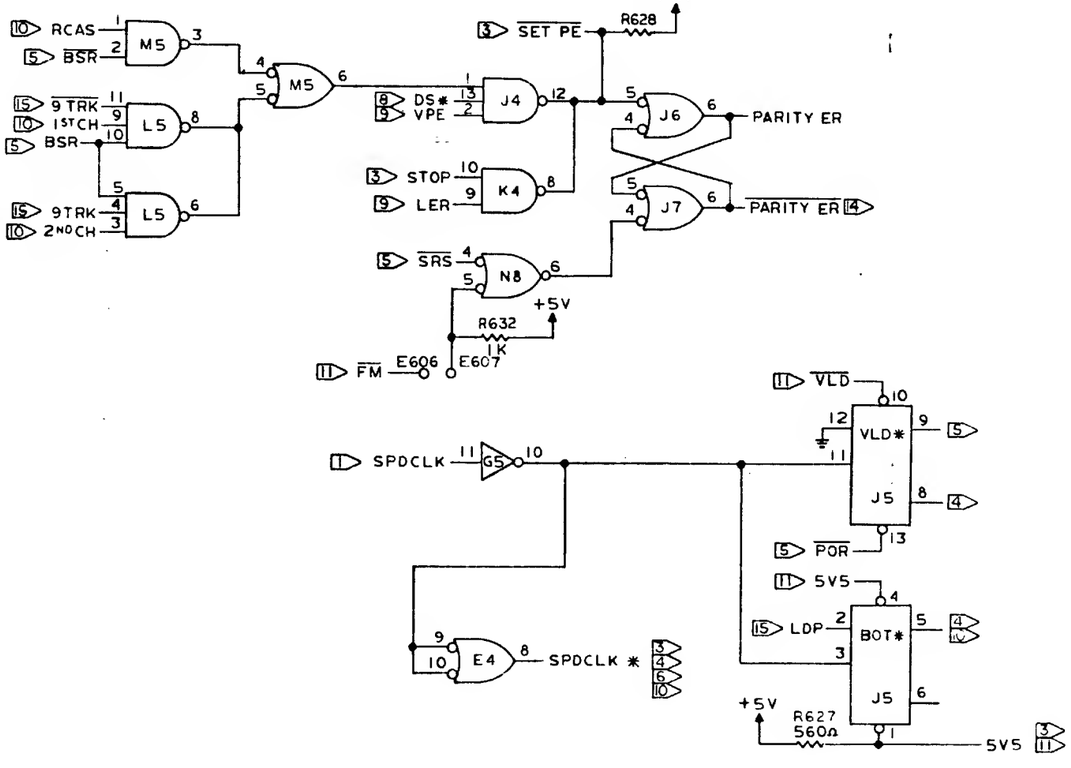
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 10 OF 16

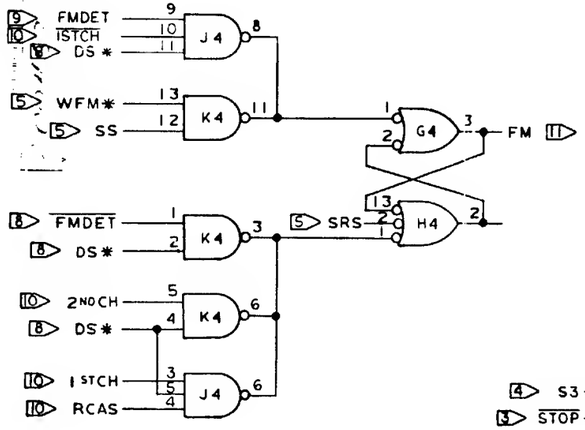
C-23

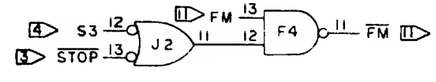
REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			









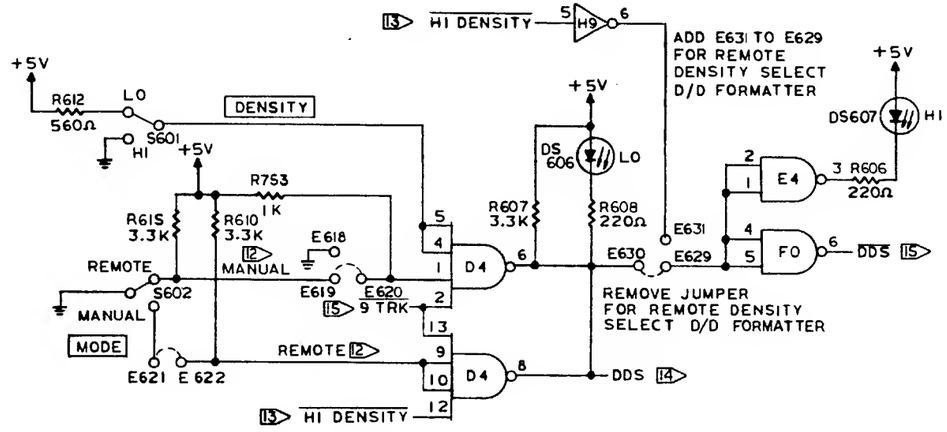


11

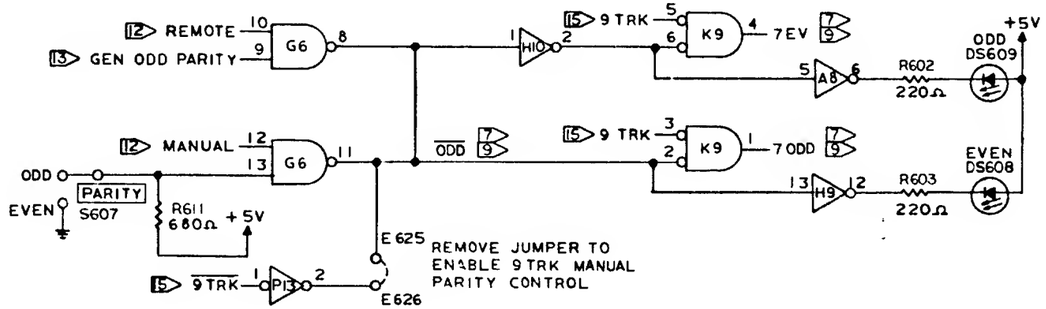
NOTES UNLESS SPECIFIED				
1. TOLERANCES XX± ANGULAR, XXX± 2	DRAWN	L AGUIRRE	4-19-79	Wangco incorporated
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK			
3. MACH. SURFACES	APPR.			CODE F 108
4. ALL DIMS IN INCHES.	MATERIAL			LOGIC SCHEMATIC NRZI FORMATTER (FORMATTER STATUS LOGIC)
	FINISH			QTY. REQ'D.
	MODEL No.		SCALE	SIZE D 200452 F
	NEXT ASSY		DO NOT SCALE THIS DRAWING	WEIGHT SHEET 11 OF 16

C-25

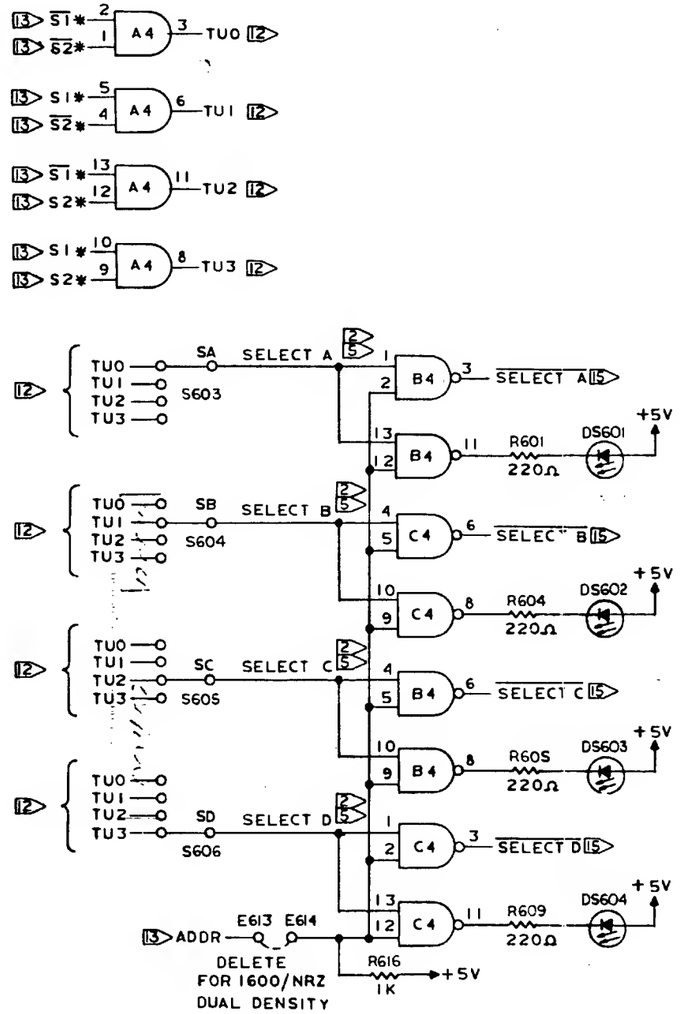
REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			



HI/LO DENSITY SELECT



PARITY CONTROL



UNIT SELECT

(12)

NOTES UNLESS SPECIFIED			
1. TOLERANCES XX± ANGULAR XXX± ±	DRAWN	L. AGUIRRE	4.19.73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(OCP LOGIC)

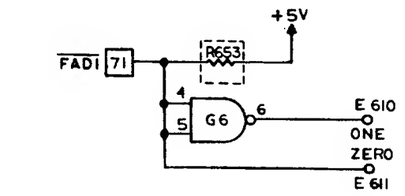
CODE F 108 | REV. RECD.

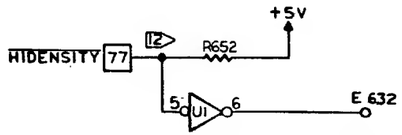
SCALE | SIZE D | 200452 | F

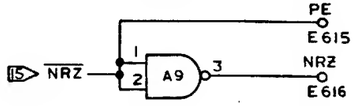
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 12 OF 16

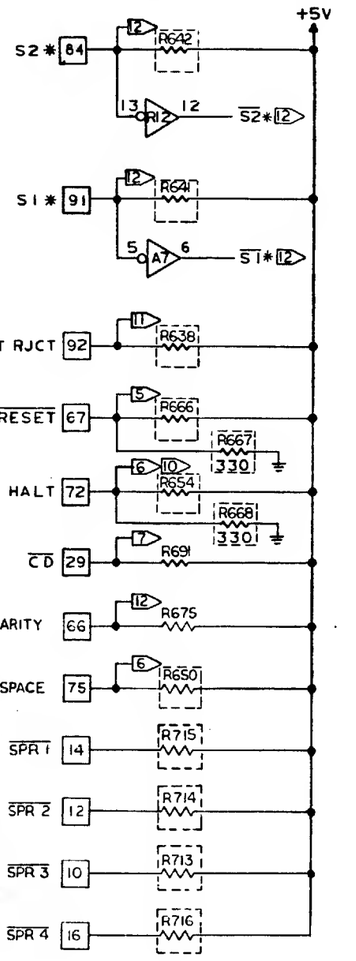
C-27

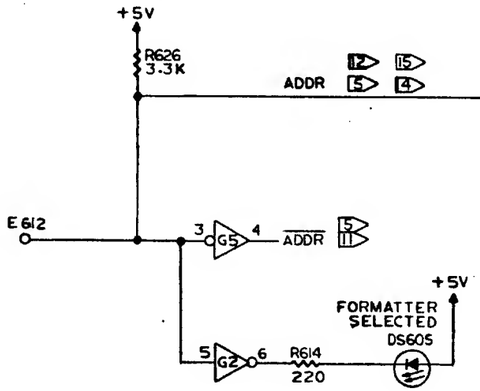
REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

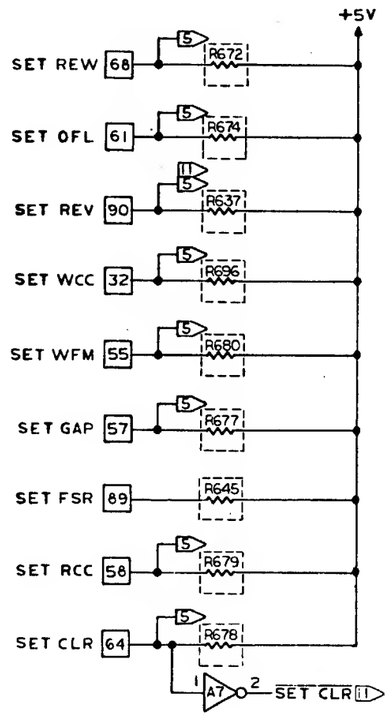


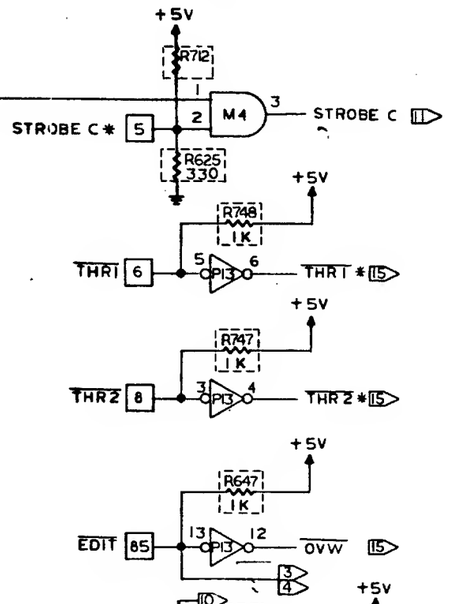












3. ALL RESISTOR [ ] ARE DELETED ON DUAL DENSITY.
2. ALL PINS [ ] ARE ON CONN'S J2, J4, J5, J101.
1. ALL RESISTORS ARE 220Ω, 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.

(13)

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L AGUILAR	4-23-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES ✓	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(COMPUTER ADAPTER TO FORMATTER INTERFACE)

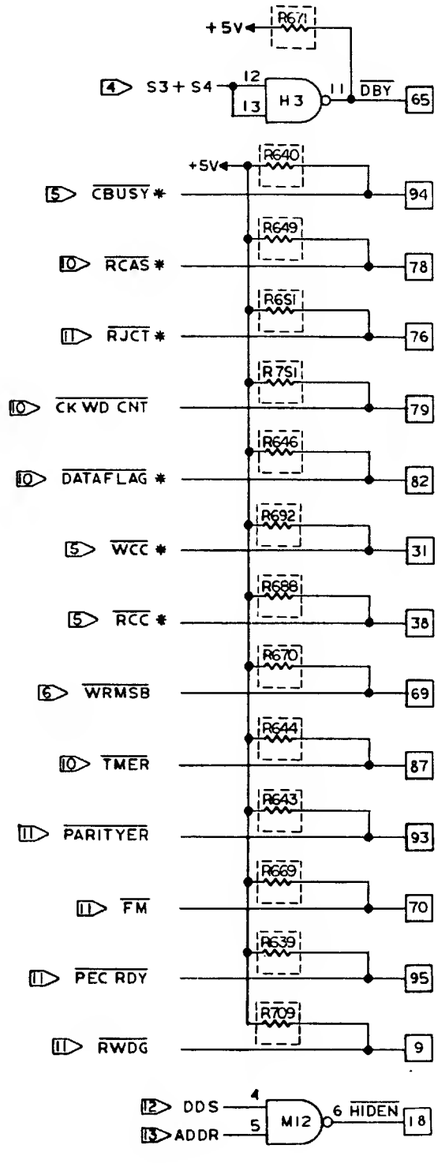
CODE F 108 | QTY. REQ'D.

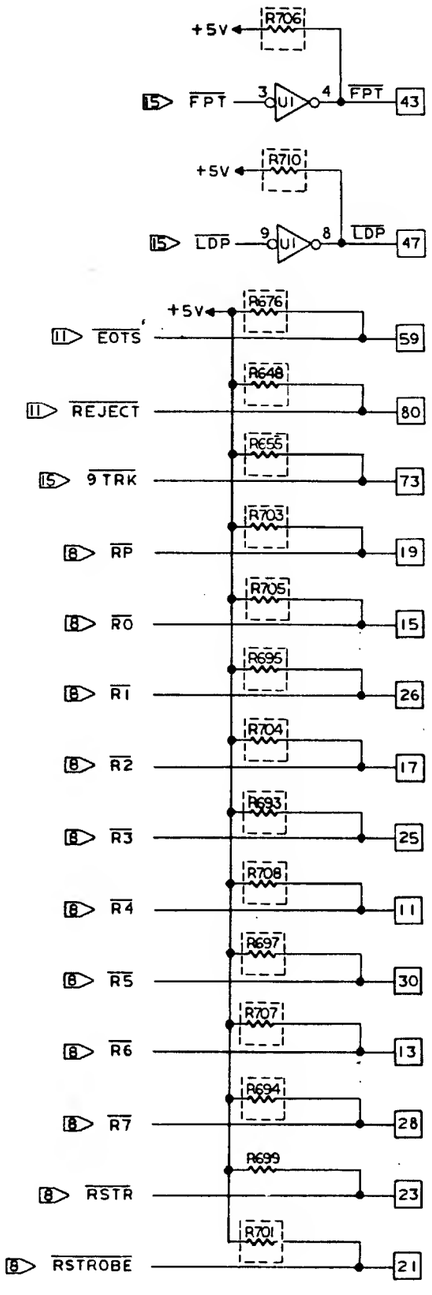
SCALE	SIZE		
	D	200452	F
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 13 OF 16	

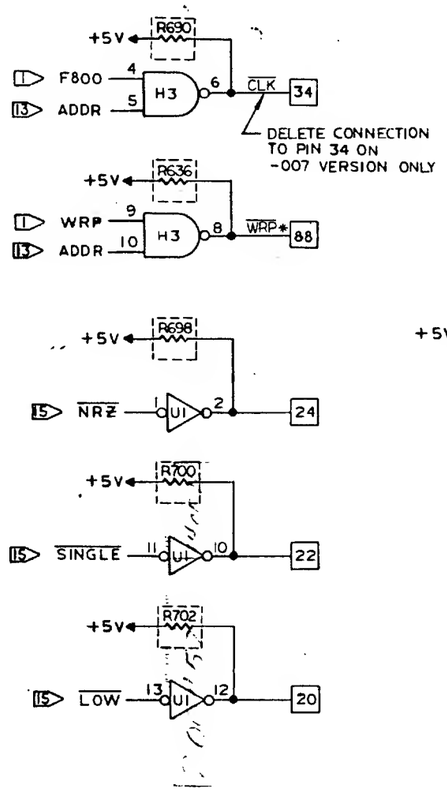
C-29

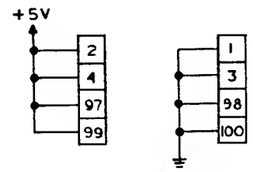
LOGIC SCHEMATIC FORMATTER

REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			









+5V UNREG — 96 | 5

3. ALL RESISTORS [ ] ARE DELETED ON DUAL DENSITY.
2. ALL PINS [ ] ARE ON CONN'S J2, J4, J6, J101.
1. ALL RESISTORS ARE 1KΩ, 1/4 W, 5%, UNLESS OTHERWISE SPECIFIED.

(14)

NOTES: UNLESS OTHERWISE SPECIFIED.

NOTES UNLESS SPECIFIED				
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L. AGUIRRE	4-26-73	Wangco Incorporated
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK			
3. MACH. SURFACES ✓	APPR.			
4. ALL DIMS IN INCHES.	MATERIAL			LOGIC SCHEMATIC NRZI FORMATTER (FORMATTER TO COMPUTER ADAPTER INTERFACE)
	FINISH			CODE F 108
	MODEL No.			QTY. REQ'D.
	NEXT ASSY			SCALE — SIZE D — 200452 — F
	DO NOT SCALE THIS DRAWING			WEIGHT — SHEET 14 OF 16

LOGIC SCHEMATIC

C-31

REVISIONS				200452 F
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

WDS — 45
WARS* — 43
WDP — 40
WD0 — 48
WD1 — 50
NOT USED FOR 7 TRACK
WD2 — 51
WD3 — 49
WD4 — 52
WD5 — 37
WD6 — 38
WD7 — 42
OVW — 8
SWS — 44

RD4 — 28 — R732 330
RD5 — 30 — R730 330
RD6 — 10 — R731 330
RD7 — 12 — R744 330
R750 330
R743 330
R742 330
R741 330

SFC — 34
SRC — 56
RWC — 36
OFFC — 55
SELECT A — 60
SELECT B — 53
SELECT C — 58
SELECT D — 54
THR2* — 92
THR1* — 94
DDS — 46
SPR1 — 86
SPR2 — 88
SPR3 — 90
SPR4 — 84

RDS — 6 — R746 330
RDP — 24 — R734 330
RD0 — 14 — R740 330
RD1 — 32 — R739 330
RD2 — 18 — R728 330
RD3 — 20 — R729 330
R738 330
R737 330
R736 330
R735 330
NOT USED FOR 7 TRACK

+5V

RDY — 64 — R724
C643 330PF
ON LINE
CN LINE — 66 — R723
C644 330 PF
REWINDING — 62 — R725
EOT — 41 — R727
LDP
LDP — 57 — R726
FPT
FPT — 70 — R722
DDI — 74 — R720
NRZ — 76 — R719
SINGLE — 78 — R718
LOW — 80 — R717
R721
7TRK — 72
ADDR
A9
9 TRK
G1
9 TRK
R723 R724 R725 R726 R727 R728 R729 R730 R731 R732 R733 R734 R735 R736 R737 R738 R739 R740 R741 R742 R743 R744 R745 R746 R750 R717 R718 R719 R720 R721 R722

+5V
2 4 97 99
1 3 98 100

3. ALL RESISTORS [ ] ARE DELETED FOR DUAL DENSITY.
2. ALL PINS ◯ ARE ON CONN'S J3, J5, J102.
1. ALL RESISTORS ARE 220Ω, 1/4W, 5%.

(15)

NOTES: UNLESS OTHERWISE SPECIFIED.

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	L AGUILLE	4-2-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES	APPR.		
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.		
	NEXT ASSY		

Wangco Incorporated

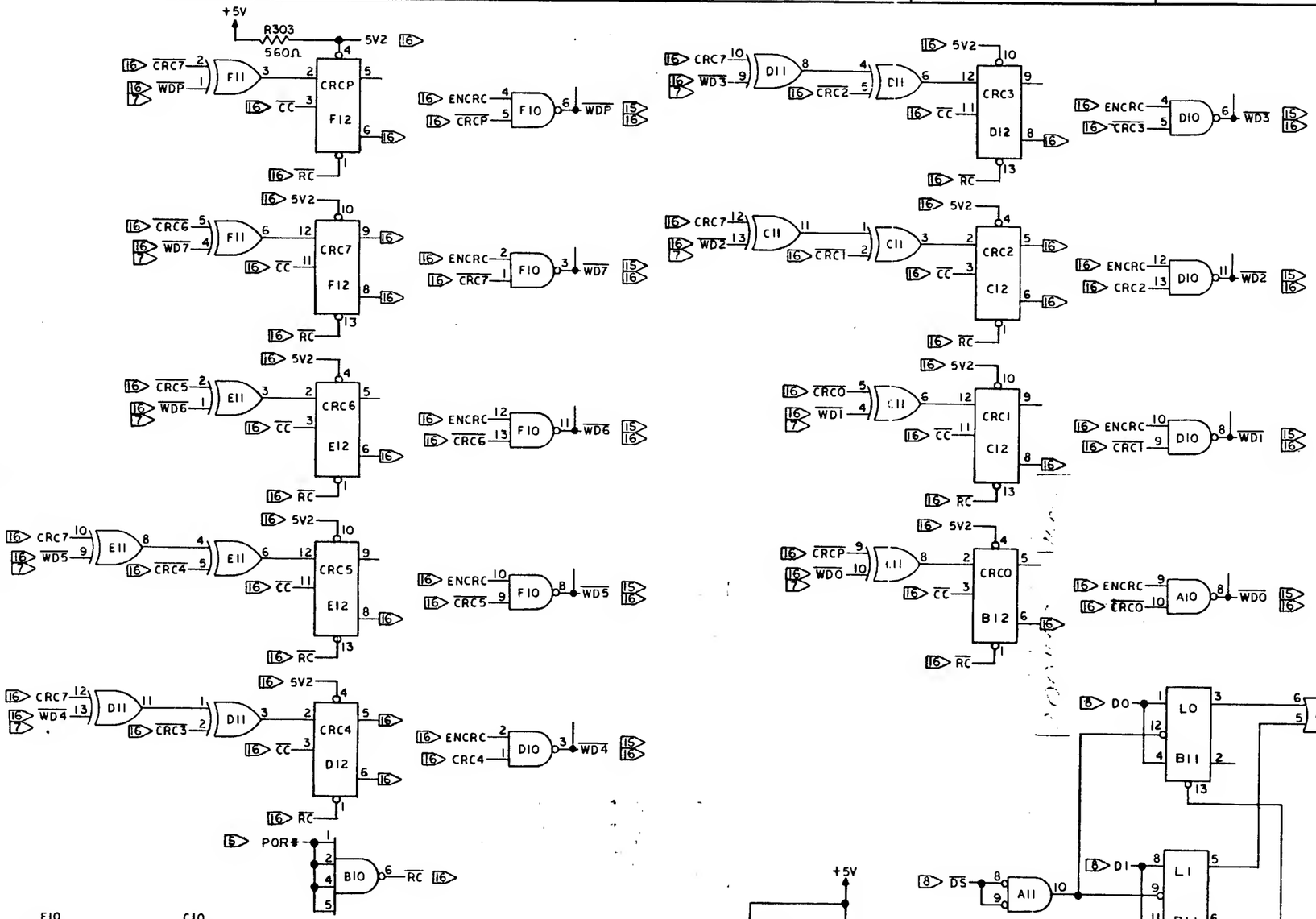
LOGIC SCHEMATIC
NRZI FORMATTER
(FORMATTER-MTU-INTERFACE)

CODE 105 — QTY. REQ'D.

SCALE — SIZE D — 200452 — F

DO NOT SCALE THIS DRAWING — WEIGHT — SHEET 15 OF 16

C-33



E10		C10	
PIN	TERM	PIN	TERM
1		1	$\overline{WD5}$
2		2	WCLP*
3	$\overline{WD7}$	3	$\overline{CC2}$
4	$\overline{WD6}$	4	
5	$\overline{WDP}$	5	CC1
6	$\overline{WD5}$	6	POR*
7	GND	7	GND
8	$\overline{WD1}$	8	D1
9	$\overline{WD3}$	9	DO
10		10	$\overline{DS}$
11	$\overline{WD2}$	11	$\overline{LER}$
12	$\overline{WD4}$	12	$\overline{S3}$
13	$\overline{WDO}$	13	$\overline{ENCRC}$
14	+5V	14	+5V

REVISIONS				200452
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHT 1			

NOTES UNLESS SPECIFIED
1. TOLERANCES XX± ANGULAR XXX± ±
2. BREAK ALL SHARP EDGES APPROX. .010
3. MACH. SURFACES
4. ALL DIMS IN INCHES.

DRAWN	L. AGUIRRE	4-25-73
CHECK		
APPR.		
MATERIAL		
FINISH		
MODEL No.		
NEXT ASSY		

Wangco Incorporated

LOGIC SCHEMATIC
NRZI FORMATTER
(CRC GENERATOR)

CODE 7 108
STK REQ'D.

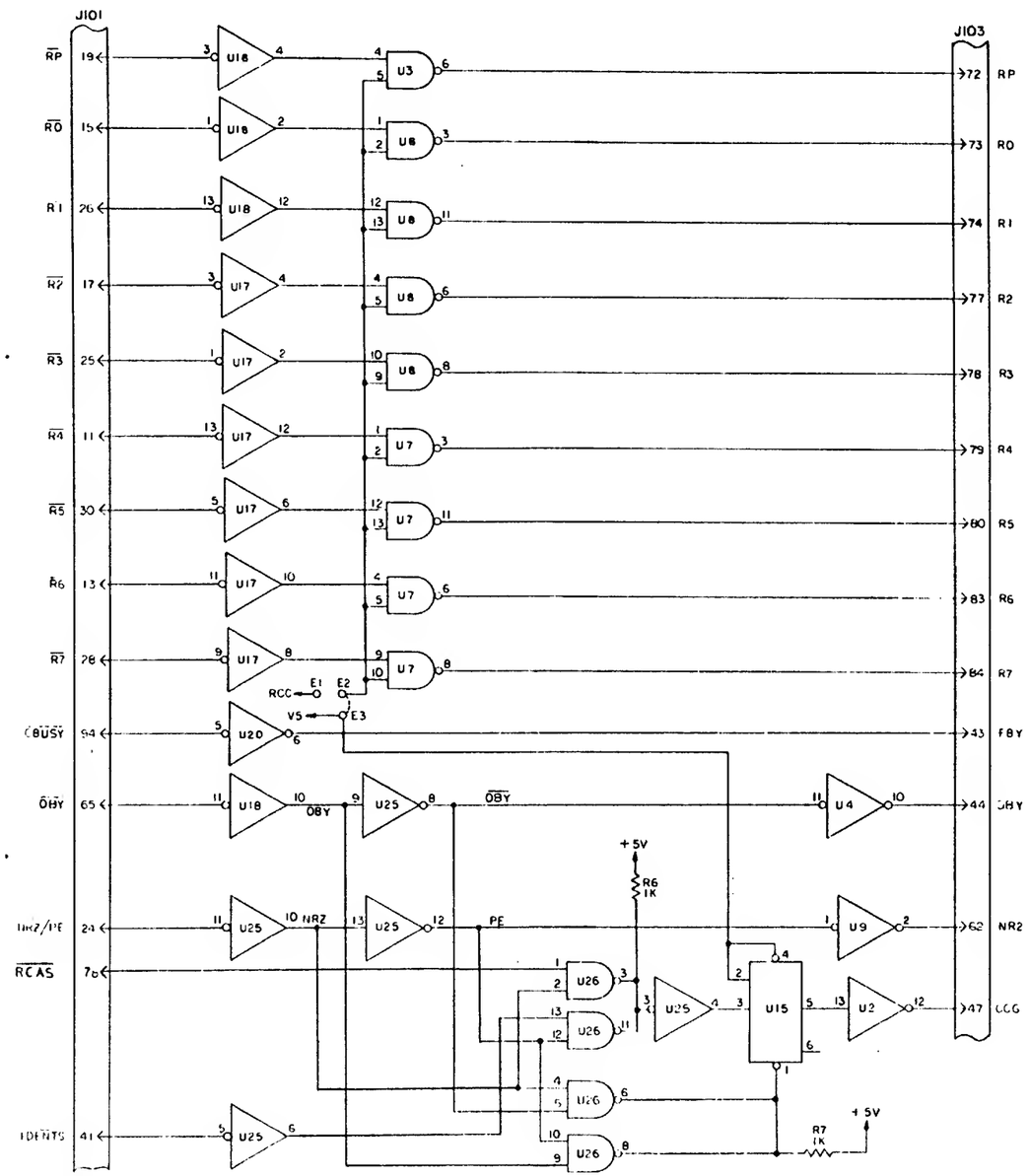
SCALE | SIZE D | 200452 | F

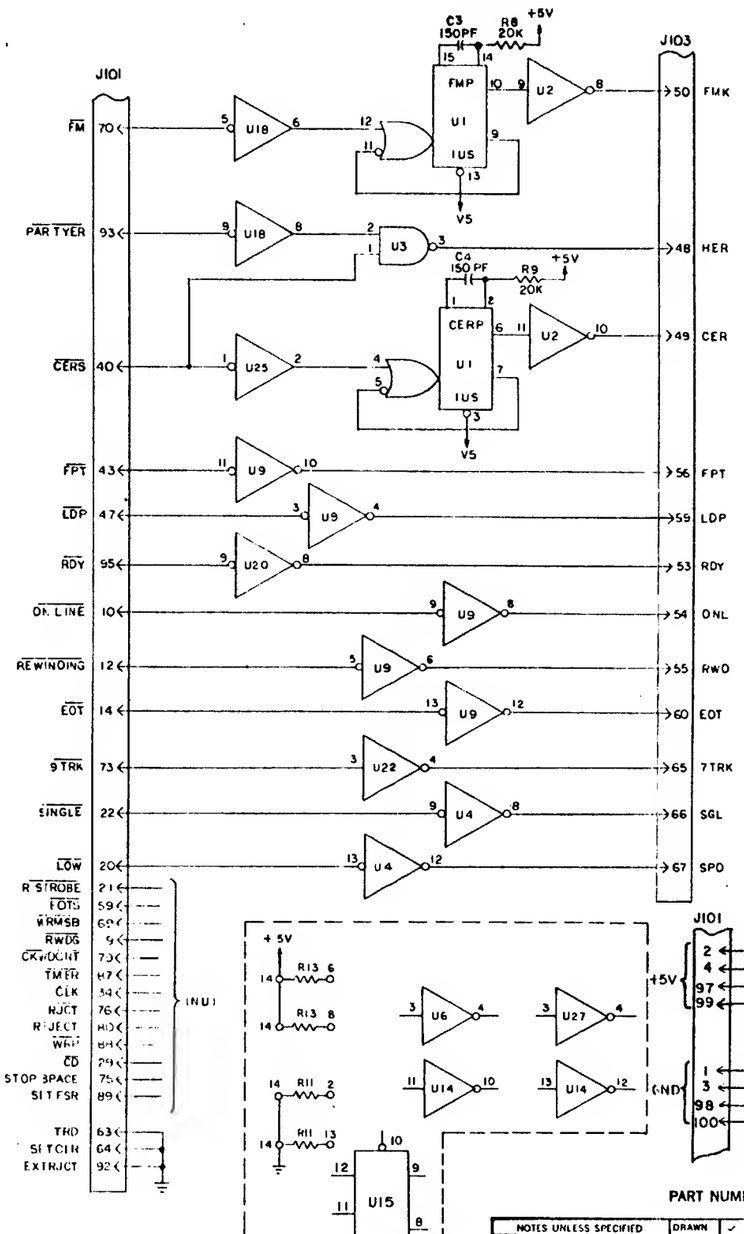
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 16 OF 16

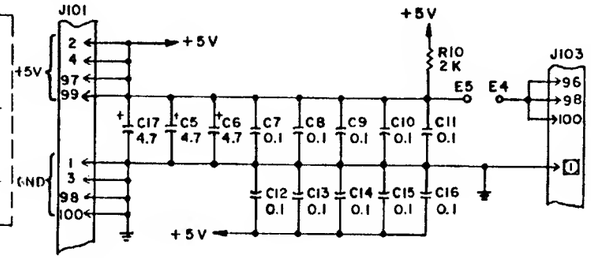
C-35

LOGIC SCHEMATIC NRZI FORMATTER

REVISIONS				202234 C
REV.	DESCRIPTION	CHK.	DATE	APPROVED
C	CR/O 7224		7/11	







DESIGNATIONS	
LAST USED	DELETED
U27	U5 U10 U16 U21
C17	
R14	

PART NUMBER

5. R13, R14 ARE 220Ω, 1/8W.
4. R11, R12 ARE 330Ω, 1/8 W.
3. ALL CAPACITORS IN MICROFARADS
2. ALL RESISTORS IN OHMS, 5%, 1/4 W.

[1] J103 - PINS 3,4,9,10,15,16,21,22,27,28,33,34,39,40,45, 46,51,52,57,58,64,69,70,75,76,81,82,95,97,99

NOTES: UNLESS OTHERWISE SPECIFIED

NOTES UNLESS SPECIFIED		
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK	
3. MACH SURFACES ✓	APVR	
4. ALL DIMS IN INCHES	MATERIAL	
5. DIMENSIONS APPLY AFTER FINISH AND HEAT TREAT	FINISH	
	MODEL No. TYPE P	
	NEXT ASSY 202233	

WANGCO INCORPORATED

SCHEMATIC
EMULATOR TYPE P

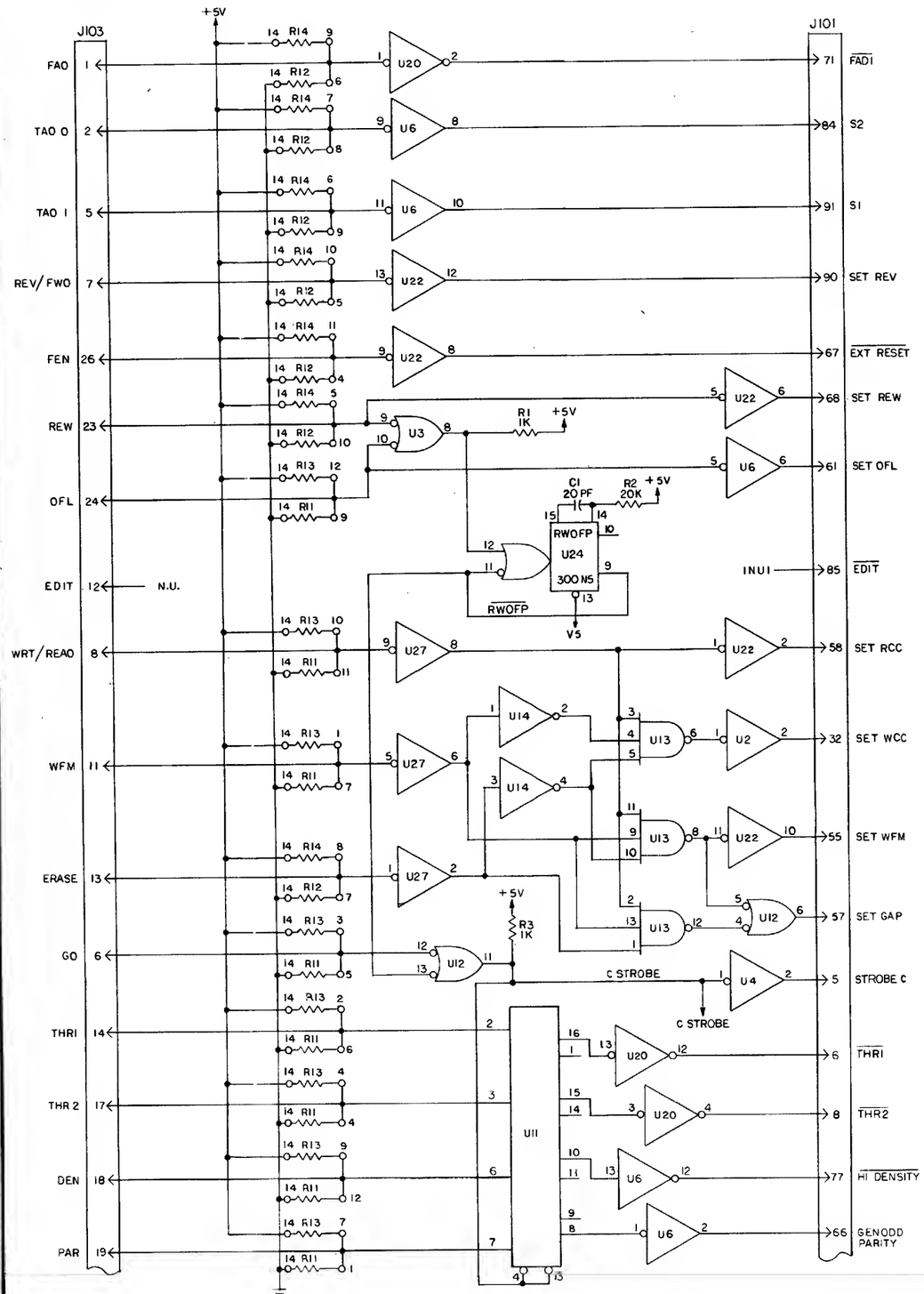
CAGE F 108 DWG. NO.

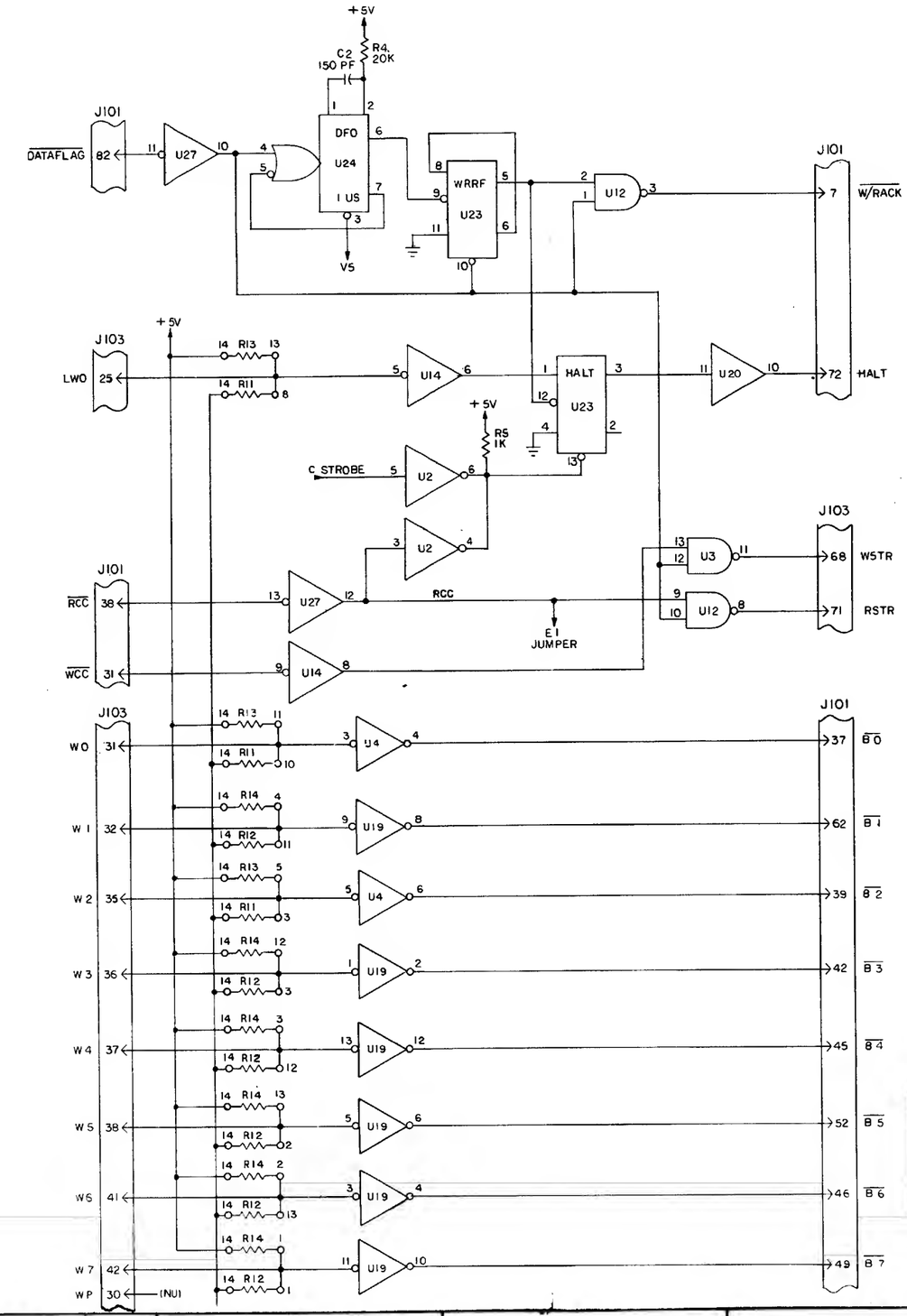
SCALE —— SIZE D 202234 C

DO NOT SCALE THIS DRAWING WEIGHT SHEET 1 OF 2

C-37

REVISIONS			202234 C
REV.	DESCRIPTION	CHK.	DATE APPROVED
—	SEE SHEET 1		





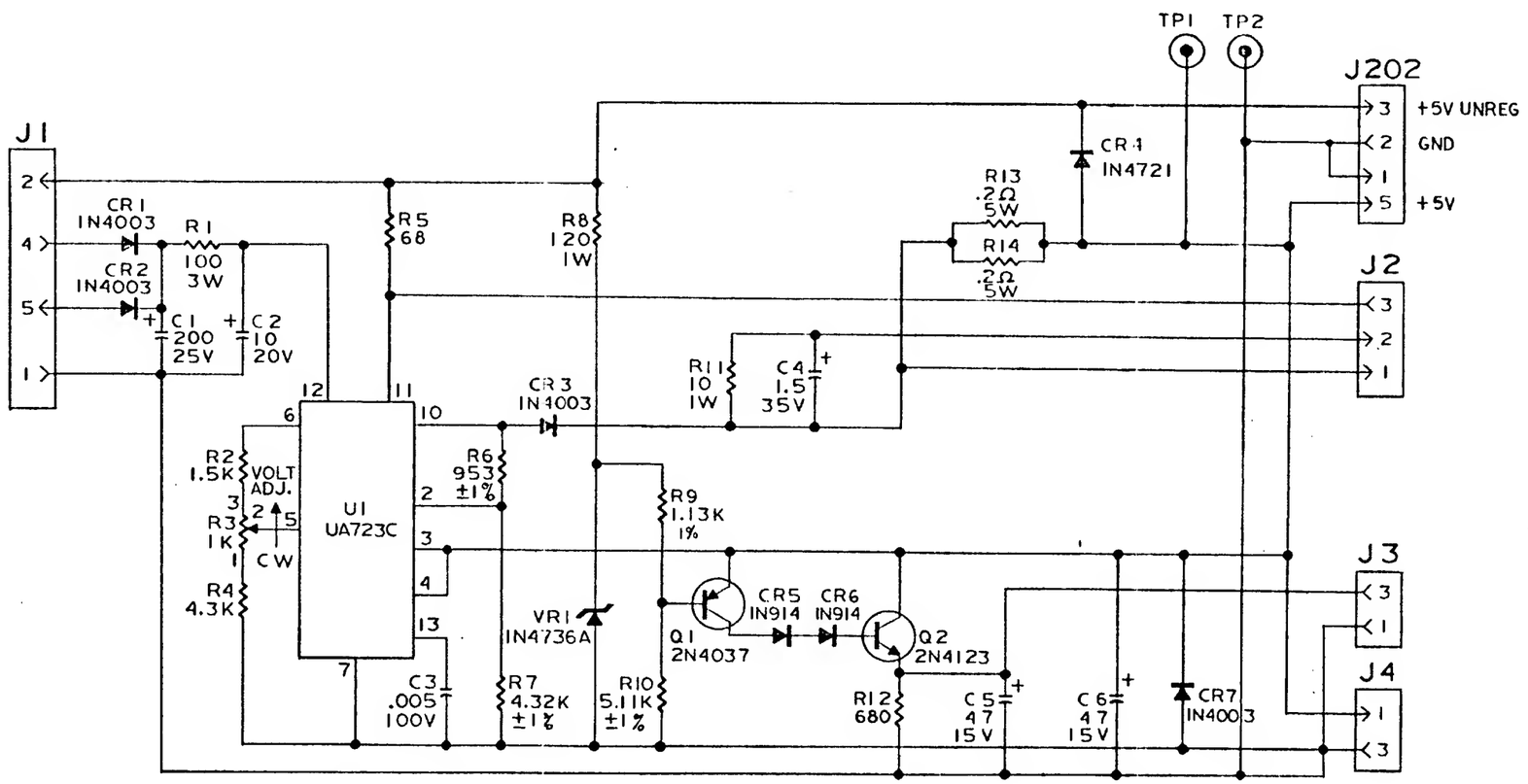
WANGCO INCORPORATED

SCHEMATIC
EMULATOR TYPE P

CODE F 108 DWG. NO.

SCALE	SIZE		
—	D	202234	C
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 2 OF 2	

REVISIONS				201562 C
REV.	DESCRIPTION	CHK.	DATE	APPROVED
—	SEE SHEET 4 OF 4		3/73	



2. ALL CAPACITORS IN MICROFARADS.
1. ALL RESISTORS IN OHMS ± 5% ¼ W.

NOTES: UNLESS OTHERWISE SPECIFIED.

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR ± .XXX± ±	DRAWN	L. AGUIRRE	1-11-73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.		1-15-73
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER	
	NEXT ASSY		

Wangco Incorporated

SCHEMATIC

POWER SUPPLY PWB

CODE F 108 | QTY. REQ'D.

SCALE	SIZE		
—	C	201562	C
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 3 OF 4	

REVISIONS				201581 F
REV.	DESCRIPTION	CHK.	DATE	APPROVED
	SEE SHEET 4			

Sch Pwr Sup Assy

PWB ASSY 201562

TB202 · B101-1 · B101-2 · 115VAC · S101 · F201 1.5A SB · TB1 · TB201 · AC IN · GND · AC RTN · BLK · GND · WHT · LINE A · LINE B · GRAY 125V · VIOLET 120V · BLUE 10V · GREEN 0V · YELLOW 125V · ORANGE 120V · RED 10V · BROWN 0V · T1 · BLK SHIELD · CR1 IN3208 · CR2 IN3208 · F202 10A · +5V UNREG · C2 65,000 20V · C1 200 25V · GND · +5V

SCR1 2N3668 · P3 J3 · Q2 2N3771 · P2 J2 · Q1 TIP30 · P1 J1 · CR1 IN4003 · CR2 IN4003 · R1 100 3W · R2 1.5K VOLT ADJ. · R3 1K CW · R4 4.32K · U1 UA723C · R5 68 · R8 120 1W · R11 10 1W · C4 1.5 35V · CR3 IN4003 · R6 953 ±1% · R9 1.13K 1% · Q1 2N4037 · CR5 IN914 · CR6 IN914 · Q2 2N4123 · VR1 IN4736A · R7 4.32K ±1% · R 0 5.11K ±1% · C3 .005 100V · R12 680 · C5 47 15V · C6 47 15V · CR7 IN4003 · R13 .2 5W · R14 .2 5W · CR3 IN7421 · J202 · P202 · +5V UNREG · GND · +5V · OPTIONAL GND WIRE · TP1 +5V · TP2 GND · J4 · P4

TABLE I
-001 VERSION

LINE VOLTAGE	TB1-1 BRN	TB1-2 GRN	TB1-3 RED	TB1-4 BLU	TB1-5 OR	TB1-6 VIO	TB1-7 YEL	TB1-8 GRY
100			LINE B	JUMPER TO 3	LINE A	JUMPER TO 5		
110			LINE B	JUMPER TO 3	LINE A	JUMPER TO 5		
115			LINE B	JUMPER TO 3			LINE A	JUMPER TO 7
120	LINE B	JUMPER TO 1			LINE A	JUMPER TO 5		
125	LINE B	JUMPER TO 1					LINE A	JUMPER TO 7
220			LINE B	JUMPER TO 5		LINE A		
230			LINE B	JUMPER TO 7				LINE A
240	LINE B	JUMPER TO 5				LINE A		
250	LINE B	JUMPER TO 7						LINE A

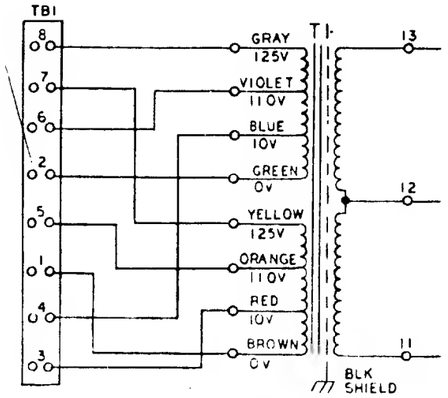


TABLE II
-002 VERSION

LINE VOLTAGE	TB1-1 BRN	TB1-2 GRN	TB1-3 RED	TB1-4 BLU	TB1-5 ORN	TB1-6 VIO	TB-7 YEL	TB1-8 GRY
100			LINE B	JUMPER TO 3	LINE A	JUMPER TO 5		
110	LINE B	JUMPER TO 1			LINE A	JUMPER TO 5		
115			LINE B	JUMPER TO 3			LINE A	JUMPER TO 7
125	LINE B	JUMPER TO 1					LINE A	JUMPER TO 7
200			LINE B	JUMPER TO 5		LINE A		
220	LINE B	JUMPER TO 5				LINE A		
230			LINE B	JUMPER TO 7				LINE A
250	LINE	JUMPER TO 7						LINE A

[3] TB1 WIRING ON F/D SHOWN AS 115V(-001)CONF SEE TABLE I, FOR -002 VERSION SEE TABLE II.

2. ALL CAPACITORS IN MICROFARADS.

1. ALL RESISTORS IN OHMS ± 5% 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

~~[4] FOR LINE VOLTAGE 100V-125V F201 IS 1.5A, 200V-250V F201 IS 0.75A~~

NOTES UNLESS SPECIFIED
1. TOLERANCES XXX ANGULAR XXXX ±
2. BREAK ALL SHARP EDGES APPROX. .010
3. MACH. SURFACES
4. ALL DIMS IN INCHES.

DRAWN · CHECK · APPR. · MATERIAL · FINISH · MODEL No. FORMATTER · NEXT ASSY

Wangco Incorporated

SCHEMATIC

POWER SUPPLY ASSEMBLY

SCALE · SIZE D · 201581 · F · DO NOT SCALE THIS DRAWING · WEIGHT · SHEET 5 OF 5

C-43

REVISIONS			201759	A
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	Manufacturing Released.		5/	

Abbreviations:- Mech. = Mechanical Connection.

Sol. = Solder Connection.

40 = Mechanical Hardware or Electrical Part. The No. is the item No. on the Material List. The circle indicates that you need this part in addition to any wire.

35 = Uncircled numbers usually indicate wire type only. The No. is also the item No. on the Material List.

C-45

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	D.Morgan.	5/21/73
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES √	APPR.		5/21/73
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	Formatter.	
	NEXT ASSY	201581	

Wangco Incorporated

LIST, WIRE.

FORMATTER POWER SUPPLY.

CODE 107

QTY. REQ'D. 1

SCALE	SIZE		
	A	201759	A
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 1 of 3	

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
1		T1 - Brown.	TB1-1	(40)				A
2		T1 - Green.	TB1-2	"				
3		T1 - Red.	TB1-3	"				
4		T1 - Blue.	TB1-4	"				
5		T1 - Orange.	TB1-5	"				
6		T1 - Violet.	TB1-6	"				
7		T1 - Yellow.	TB1-7	"				
8		T1 - Gray.	TB1-8	"				
9		T1 - Black.	Chassis Ground	"				
10	Mech.	TB1-3	TB1-4	(29)				
11	"	TB1-7	TB1-8	"				
12		T1-11	CR2 Anode	Sol.				
13	Sol.	CR-2 Anode	P1-5	(33)	58			
14		T1-12	C2-Neg.	(39)				
15	(41)	C2-Neg.	P1-1	(34)	58			
16		T1-13	CR1 Anode.	Sol.				
17	Sol.	CR1 Anode.	P1-4	(34)	58			
18	Sol.	CR1 Cathode.	CR2 Cathode.	Sol.	55			
19	"	CR1 Cathode	C2-Positive	(39)	56			
20	"	Q1 Emitter	Q2 Collector	(42)	58			
21	(40)	Q2 Collector	SCR1 Anode	(40)	58			
22	Sol.	Q1 Base	P2-3	(34)	58			
23	(40)	Q1 Collector.	Q2 Base.	Sol	58			
24	(40)	Q1 Collector.	P2-2	(33)	58			
25	Sol.	Q2 Emitter	P2-1	(33)	58			
26	"	SCR1 Gate.	P3-3	(34)	58			A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE
FORMATTER POWER SUPPLY.

Wang Computer Products

201759 A

SHEET 2 OF 3

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
27	Sol.	SCR1 Cathode.	P3-1	(33)	58			A
28	(40)	SCR1 Anode.	P1-2	(33)	58			
29	(40)	TB1-4	TB202-4	(40)	58			
30	(40)	TB1-7	TB202-2	(40)	58			
31	(40)	TB1-8	TB202-3	(40)	58			
32	(40)	TB202-5	P4-3	(34)	58			
33	(40)	TB202-6	P4-1	(33)	58			
34	Sol	F202-2	C2 Positive.	(39)	57			
35	"	F202-1	SCR1 Anode	(38)	57			
36	"	F201-2	TB201-1	Sol	58			
37	"	F201-1	TB202-1	(40)	58			
38	"	Tb201-2	TF1-3	(40)	58			
39	"	B101-1	TB202-3	(40)	59	Twisted Pair.		
40	"	B101-2	TB202-4	(40)	59	Black/Red.		A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

FORMATTER POWER SUPPLY.

Wang Computer Products

201759 A

SHEET 3 OF 3

REVISIONS			201337	A
REV.	DESCRIPTION	CHK.	DATE	APPROVED
A	Manufacturing Release	[illegible]	8/29/72	[illegible]

C-49

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX± ANGULAR .XXX± ±	DRAWN	G. Scott	8/29/72
2. BREAK ALL SHARP EDGES APPROX. .010	CHECK		
3. MACH. SURFACES ✓	APPR.	[illegible]	8/29/72
4. ALL DIMS IN INCHES.	MATERIAL		
	FINISH		
	MODEL No.	FORMATTER	
	NEXT ASSY	201336	

Wang Computer Products

LIST, CABLE WIRING

MTU TO FORMATTER

CODE

QTY. REQ'D. 1

SCALE	SIZE		
	A	201337	A

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 1 of 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
1	Sol	P16 -A	P102 -80	Sol	(10)	Brown } Tw. Pr.	$\overline{\text{LOW}}$/HIGH SPD	A
2		-1	-Gnd			Black }	GND	
3		-B	-8			Red }	$\overline{\text{OWW}}$	
4		-2	-Gnd			Black }	GND	
5		-C	-34			Orange }	$\overline{\text{SFC}}$	
6		-3	-Gnd			Black }	GND	
7		-D	-46			Yellow }	$\overline{\text{DDS}}$	
8		-4	-Gnd			Black }	GND	
9		-E	-56			Green }	$\overline{\text{SRC}}$	
10		-5	-Gnd			Black }	GND	
11		-F	-74			Blue }	$\overline{\text{DDI}}$	
12		-6	-Gnd			Black }	GND	
13		-H	-36			Violet }	$\overline{\text{RWC}}$	
14		-7	-58			Black }	$\overline{\text{SELECT C}}$ (SEL 2)	
15		-J	-60			Gray }	$\overline{\text{SELECT A}}$ (SEL 0)	
16		-8	-53			Black }	$\overline{\text{SELECT B}}$ (SEL 1)	
17		-K	-44			White }	SWS	
18		-9	-54			Black }	$\overline{\text{SELECT D}}$ (SEL 3)	
19		-L	-55			Brown }	$\overline{\text{OFFC}}$	
20		-10	-Gnd			Black }	GND	
21		-M	-66			Red }	$\overline{\text{ONLINE}}$	
22		-11	-Gnd			Black }	GND	
23		-N	-62			Orange }	$\overline{\text{RWDG}}$	
24		-12	-Gnd			Black }	GND	
25		-P	-70			Yellow }	$\overline{\text{FPT}}$	
26	Sol	P16 -13	P102 -Gnd	Sol	(10)	Black } Tw. Pr.	GND	A

C-50

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 2 OF 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
27	Sol	P16 -R	P102 -57	Sol	10	Green ⎫ Tw. Pr.	$\overline{\text{LDP}}$	A
28	Sol	-14	P102 -Gnd	Sol		Black ⎭	GND	
29	-	-S	Reserved	-		Blue ⎫ Tw. Pr.	Reserved	
30	-	-15	Reserved	-		Black ⎭	Reserved	
31	Sol	-T	P102 -64	Sol		Violet ⎫ Tw. Pr.	$\overline{\text{RDY}}$	
32		-16	-Gnd			Black ⎭	GND	
33		-U	-41			Gray ⎫ Tw. Pr.	$\overline{\text{EOT}}$	
34	Sol	-17	P102 -Gnd	Sol		Black ⎭	GND	
35		-V	(Spare)			White ⎫ Tw. Pr.	SPARE	
36		P16 -18	(Spare)		10	Black ⎭	SPARE	A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 3 OF 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
37	Sol	P1 -A	P102 -45	Sol	(10)	Brown } Tw. Pr.	$\overline{WDS}$	A
38	Sol	-1	P102 -Gnd	Sol		Black }	GND	
39		-B	(Reserved)			Red }	Reserved	
40		-2	(Reserved)			Black }	Reserved	
41	Sol	-C	P102 -43	Sol		Orange }	$\overline{WARS}$	
42		-3	-Gnd			Black }	GND	
43		-D	-92			Yellow }	$\overline{RTH2}$	
44		-4	-Gnd			Black }	GND	
45		-E	-94			Green }	$\overline{RTH1}$	
46	Sol	P1 -5	P102 -Gnd	Sol		Black }	GND	
47						Blue }	SPARE	
48						Black }	SPARE	
49		P1 -H	(Reserved)			Violet }	Reserved	
50		-7	(Spare)			Black }	SPARE	
51		-J	(Spare)			Gray }	SPARE	
52		-8	(Spare)			Black }	SPARE	
53		-K	(Reserved)			White }	Reserved	
54		-9	(Reserved)			Black }	Reserved	
55	Sol	-L	P102 -40	Sol		Brown }	$\overline{WDP}$	
56		-10	-Gnd			Black }	GND	
57		-M	-48			Red }	$\overline{WD0}$	
58		-11	-Gnd			Black }	GND	
59		-N	-50			Orange }	$\overline{WD1}$	
60		-12	-Gnd			Black }	GND	
61		-P	-51			Yellow }	$\overline{WD2}$	
62	Sol	P1 -13	P102 -Gnd	Sol	(10)	Black } Tw. Pr.	GND	A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 4 OF 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
63	Sol	P1 -R	P102 -49	Sol	10	Green } Tw. Pr.	$\overline{WD3}$	A
64		-14	-Gnd			Black }	GND	
65		-S	-52			Blue }	$\overline{WD4}$	
66		-15	-Gnd			Black }	GND	
67		-T	-37			Violet }	$\overline{WD5}$	
68		-16	-Gnd			Black }	GND	
69		-U	-38			Gray }	$\overline{WD6}$	
70		-17	-Gnd			Black }	GND	
71		-V	-42			White }	$\overline{WD7}$	
72	Sol	P1 -18	P102 -Gnd	Sol	10	Black } Tw. Pr	GND	A
73	Sol	P1 -D	P1 -F	Sol	11		$\overline{RTH2}$	A
74	Sol	P1 -4	P1 -6	Sol	11		GND	A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 5 OF 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
75	Sol	P6 -1	P102 -24	Sol	(10)	Brown Tw. Pr.	$\overline{RDP}$	A
76		-A	-Gnd			Black	GND	
77		-2	-6			Red	$\overline{RDS}$	
78		-B	-Gnd			Black	GND	
79		-3	-14			Orange	$\overline{RD0}$	
80		-C	-Gnd			Black	GND	
81		-4	-32			Yellow	$\overline{RD1}$	
82	Sol	-D	P102 -Gnd	Sol		Black	GND	
83		-5	(Spare)			Green	SPARE	
84		-E	(Spare)			Black	SPARE	
85	Sol	-6	P102 -78	Sol		Blue	$\overline{SINGLE}$/DUAL	
86	Sol	-F	P102 -Gnd	Sol		Black	GND	
87		-7	(Spare)			Violet	SPARE	
88		-H	(Spare)			Black	SPARE	
89	Sol	-8	P102 -18	Sol		Gray	$\overline{RD2}$	
90		-J	-Gnd			Black	GND	
91		-9	-20			White	$\overline{RD3}$	
92		-K	-Gnd			Black	GND	
93		-10	-76			Brown	$\overline{NRZ}$/PE	
94		-L	-Gnd			Black	GND	
95		-11	-72			Red	$\overline{7\ TRK}$/9 TRK	
96	Sol	-M	P102 -Gnd	Sol		Black	GND	
97		-12	(Spare)			Orange	SPARE	
98		-N	(Spare)			Black	SPARE	
99		-13	(Spare)			Yellow	SPARE	
100		P6 -P	(Spare)		(10)	Black Tw. Pr.	SPARE	A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 6 OF 7

Wire No.	Term.	From	To	Term.	Wire Type	Notes	Signal	Chg Let.
101	Sol	P6 -14	P102 -28	Sol	10	Green } Tw. Pr.	$\overline{RD4}$	A
102	↕	↕ -R	↕ -Gnd	↕	↕	Black } ↕	GND	↕
103	↕	↕ -15	↕ -30	↕	↕	Blue } ↕	$\overline{RD5}$	↕
104	Sol	-S	P102 -Gnd	Sol		Black }	GND	
105		-16	(Spare)			Violet }	SPARE	
106		-T	(Spare)			Black }	SPARE	
107	Sol	-17	P102 -10	Sol		Gray }	$\overline{RD6}$	
108	↕	↕ -U	↕ -Gnd	↕		Black }	GND	
109	↕	↕ -18	↕ -12	↕	↕	White } ↕	$\overline{RD7}$	↕
110	Sol	P6 -V	P102 -Gnd	Sol	10	Black } Tw. Pr.	GND	A

1. Ref item no's in applicable material list
2. Ref designations are abbreviated
   Prefix each designation with

TITLE

LIST, WIRE

Wang Computer Products

201337 A

SHEET 7 OF 7